UNIVERSIDADE FEDERAL DE SÃO CARLOS

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NanOLaB

A study of SnO2 nanowire FET devices: ambipolarity effect induced by UV Light exposure and their use as UV sensors.

Adryelle do Nascimento Arantes

Advisor: Prof. Dr. Adenilson José Chiquito

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Thesis presented to Universidade Federal de São Carlos, as a partial requisition to obtain the master's degree in Physics.

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4. ARANTES, A. N.; DE ARAÚJO, E. P. ; PELLEGRINI, M. ; PEDERSOLI, A. A. ; CHIQUITO, A. J. *A simple band model for ultraviolet induced ambipolarity in single SnO2 nanowire devices.* PHYSICA E-LOW-DIMENSIONAL SYSTEMS & NANOSTRUCTURES, v. 128, p. 114607, 2020.

Abstract

In this work, SnO$_2$ nanowires (NW) were grown by the Vapor-Liquid-Solid (VLS) method and used to build single NW FET devices. As-grown samples went through structural and morphological analysis and seven single NW devices were built, with a back-gated FET architecture, by direct photolithography. SnO$_2$ NWs grown by VLS method presented the desired tetragonal structure and monocrystalline character, inspected by XRD and HRTEM techniques. In addition, the as-grown samples morphology of a NW with lengths of tens of micrometers and cross-section mostly displaying rectangular geometry were assured through SEM images. The device fabrication process by direct photolithography was proven to be efficient to build the back-gated FET architecture devices with great electrical contacts quality. Single SnO2NWFET's transport properties were explored, where on/off ratio, mobility and carrier density parameters were extracted, resulting in values around 10^5, lower than 0.1 cm^2/V and in the order of 10^{19}/cm^3, respectively. Schottky barrier heights were estimated, considering the gate bias as grounded and room temperature, and Φ_{Bn} values between 0.41 and 0.75 eV were found. Afterwards, different conditions were analyzed: the device (1) under positive gate bias ($V_G > 0$) and no applied source/drain bias ($V_{DS} = 0$); (2) $V_{DS} > 0$ and $V_G > 0$; (3) $V_{DS} < 0$ and $V_G < 0$ and (4) $V_{DS} < 0$, $V_G < 0$ but under UV illumination. Regarding the latter, all devices presented UV induced ambipolary effect, where on/off states ratio with values of the same order were obtained and ranged from 1.1 to about 19.3. A simple band model to explain the observed behavior, i.e., describe how both types of carriers can contribute to the final current depending on the biasing was proposed. Ambipolarity is one of those effects that may direct its use for specific purposes, where a controllable separated unipolar mode can be achieved in one single device. Furthermore, the devices were tested as UV sensors and presented satisfactory results: as a UV photodetector, the acquired I_{on}/I_{off} ratio was found to be of the order of 10^4 for all devices investigated. In addition, rise time was found to range 0.56 s < τ_r < 0.63 s, whereas the decay time 0.54 s < τ_d < 0.75 s. According to those results, one can assure their huge feasibility as a UV sensor.

Key-words: SnO$_2$ single nanowire FET, SnO$_2$ nanowires, VLS growth, induced ambipolarity, UV photodetector.

Resumo

Neste trabalho, nanofios (NW, do inglês *Nanowire*) de SnO₂ foram crescidos pelo método Vapor-Líquido-Sólido (VLS) e utilizados para construir dispositivos FET (do inglês, *Field Effect Transistor*) de um único nanofio (SnO₂NWFET). As amostras crescidas passaram por análises estruturais e morfológicas e sete dispositivos foram construídos, com uma arquitetura do tipo *back-gate*, por fotolitografia direta. Os NWs de SnO₂ crescidos pelo método VLS apresentaram a estrutura tetragonal e o caráter monocristalino desejados, inspecionados pelas técnicas de difratometria de raio X (DRX) e microscopia eletrônica de transmissão de alta resolução (HRTEM). Além disso, a morfologia de NWs com comprimentos de dezenas de micrômetros e seção transversal exibindo, em geral, geometria retangular foram observadas por meio de imagens de microscopia eletrônica de varredura (MEV). O processo de fabricação do dispositivo por fotolitografia direta mostrou-se eficiente para construir dispositivos com ótima qualidade de contatos elétricos. As propriedades de transporte de SnO₂NWFET foram exploradas, onde a relação on/off, a mobilidade e os parâmetros de densidade de portadores foram extraídos, resultando em valores em torno de 10^5, menores que 0,1 cm²/V e na ordem de 10^{19}/cm³, respectivamente. Foram estimadas as alturas das barreiras Schottky, considerando o *gate* como aterrado, e foram encontrados valores de Φ_{Bn} entre 0,41 e 0,75 eV. Posteriormente, diferentes condições foram analisadas: o dispositivo (1) com tensão positiva aplicada no *gate* ($V_G > 0$), sem tensão aplicada na fonte/dreno ($V_{DS} = 0$); (2) $V_{DS} > 0$ e $V_G > 0$; (3) $V_{DS} < 0$ e $V_G < 0$ e (4) $V_{DS} < 0$, $V_G < 0$ mas sob irradiação de luz ultravioleta (UV). Em relação a este último, todos os dispositivos apresentaram efeito ambipolar induzido pela luz UV, onde foram obtidas relações de estados on/off com valores da mesma ordem que variaram de 1,1 a cerca de 19,3. Foi proposto um modelo simples de bandas para explicar o comportamento observado, ou seja, descrever como os dois tipos de portadores podem contribuir para a corrente final dependendo da polarização. A ambipolaridade é um daqueles efeitos que podem direcionar seu uso para fins específicos, onde um modo unipolar separado controlável pode ser alcançado em um único dispositivo. Além disso, os dispositivos foram testados como sensores de luz UV e apresentaram resultados satisfatórios: como fotodetector de luz UV, a relação I_{on}/I_{off} adquirida foi da ordem de 10^4 para todos os dispositivos investigados. Além disso, foi observado um tempo de subida (τ_r) 0,56

s < τ_r< 0,63, enquanto o tempo de decaimento (τ_d) 0,54 s < τ_d< 0,75 s. De acordo com esses resultados, pode-se assegurar sua enorme viabilidade como sensor UV.

Palavras-chave: FET de um único nanofio de SnO_2, nanofios de SnO_2, ambipolaridade induzida, fotodetector de luz UV.

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1.Introduction

The growing demand for solid state devices dates from the discovery of the transistor effect [1], in which the study of semiconductor materials was strongly boosted and, among applications, the use as detectors in devices based on field effect transistors (FET) has become increasingly promising. One class of interest for the constitution of these devices is the transparent conducting oxides (TCO), such as SnO_2, ZnO, In_2O_3 and ITO which, due to their physical, chemical and optical properties [2,3], demonstrate to be appropriate components of optoelectronic devices, gas detectors and biochemical sensors [4]. The most common category of FET is the MOSFET (MOS as in metal-oxide semiconductors), a frequent component of integrated circuits that, when its structure is adapted for sensing purposes, gives rise to new devices: the ion-sensitive FET (ISFET), Water gate FET (WGFET), Nanowire FET (NWFET), among others. The latter, uses nanowire (NW) as a conducting channel, which in turn is sensitive to variations in surface carriers and optical excitation [5], presenting a wide range of applications as electronic devices, gas sensors and biochemical detection [6,7] .

For about three decades [8] the development of nanotechnology has made possible to build one-dimensional structures (1D) in a well-controlled way, e.g., NWs and nanotubes, enabling the study of phenomena related to electronic transport, for instance, quantum confinement, tunneling, giant magneto resistance effects, etc. [9]. Furthermore, owing to the large surface-volume ratio, properties related to surface effects become prominent and dominant, which results in high sensitivity and selectivity when compared to thin (2D) and bulk (3D) films. Economically, the low energy consumption and compatibility with microelectronics [10] drove the development of increasingly accurate techniques.

Controlled growth techniques reported in the literature include molecular beam epitaxy (MBE), which provides control of atomic monolayers [11], pulsed layer deposition (PLD), essential for growth of films with complex stoichiometry [12], and other techniques that are more economically viable, even among the chemical vapor deposition (CVD) class, such as the VS (Vapor-Solid) and VLS (Vapor-Liquid-Solid) growth methods [13]. These methods are the most used and efficient [6], resulting in structures with high crystallinity [14].

Among TCOs, SnO_2 stands out due to its extensive research since the 1970s [15,16] and vast abundance in our country [17]. When on a nanometric scale, e.g., a NW, the large surface-to-volume ratio leads to highlighted surface effects, making it even more interesting. By deviating from its correct stoichiometry, the defects generated by Oxygen vacancies and interstitial Tin atoms modify and produce surface states and, because the NW cross-section is comparable to the Debye length (distance over which significant charge separation can occur) [2,9], its electrical properties are strongly altered when modifying the surface states. SnO_2NWFETs are extensively explored as gas sensors [6,10,18] and photodetectors [19]; however, low dimensional related effects, e.g., the influence of surface states in conduction [2,7], are not as well established as the ones that take place in bulk materials and may modify a device's operation, driving research topics in such matter.

In this work, we discuss SnO_2NWFET properties, such as output and transfer characteristics, mobility and carrier density values acquired for different devices. Furthermore, an ambipolarity effect induced by ultraviolet (UV) exposure was noticed and a simple band model for this behavior proposed. In addition to those results, SnO_2NWFET devices were briefly explored as UV photodetectors. This work is divided in four sections: the first one presents a brief introduction to the theory regarding Tin dioxide's properties, metal-semiconductor junctions, FET devices and photoconductivity; experimental details of NW's synthesis and device fabrication process; a results and discussion section, which is then divided in two parts: Single SnO_2NWFET devices and their properties, discussing the ambipolarity effect that arises from this architecture and their potential as UV detectors; and finally, the conclusion section is presented.

1.1. Goals

The basic aim of this proposal is related to the development and study of NW-based electronic devices. The specific objectives and expected results are listed below.

1. Produce NWs of SnO_2 in a controlled manner using a growth process based on chemical vapor deposition (CVD). Despite the dominance in our group of the mentioned growth process, the present proposal requires different types of structures that can be obtained acting during the growth process. For example, the production of NWs with specific sizes and in specific regions of a device that will define the sensor element;

2. Choice and production of the sensor device in the desired architecture. The one considered in this proposal is a single-NW FET device, with a back-gate architecture and active control (variable applied voltage on the gate).

3. Study of single-NW FET devices and propose a model to understand the behavior of an ambipolar device.

4. Study of single-NW FET devices and their response as UV photodetectors.

2. Theory

This chapter will present fundamental Tin dioxide's properties, regarding its structure, optical and electrical characteristics and applicability as components of detection devices. As means to understand a FET device's operation, the following topics will discuss the metal-semiconductor junction and FET theories. In addition, the latter will also approach NW based devices, highlighting some expected results and a different operation mode that can arise from this architecture, e.g., the ambipolar behavior. Lastly, the photoconductivity effect and results expected for a semiconductor will conclude the chapter.

2.1. Tin Dioxide

Tin dioxide (SnO_2) based devices have been extensively studied since the 70s due to its huge applicability, for instance, in optical electronic devices, solar cells, liquid crystal displays, gas and biochemical sensors [2-3]. It is classified as a transparent conducting oxide (TCO) and combines high conductivity, high transparency in the visible region, mechanical, thermal and chemical stability. It is commercially found as a whitish powder [Figure 1 (a)] and shows a tetragonal structure (rutile type). As the unit cell depicts [Figure 1 (b)], it is composed by 2 Tin (Sn) atoms and 4 Oxygen (O) atoms, in which the gray atoms represent Sn and the red atoms represent O.
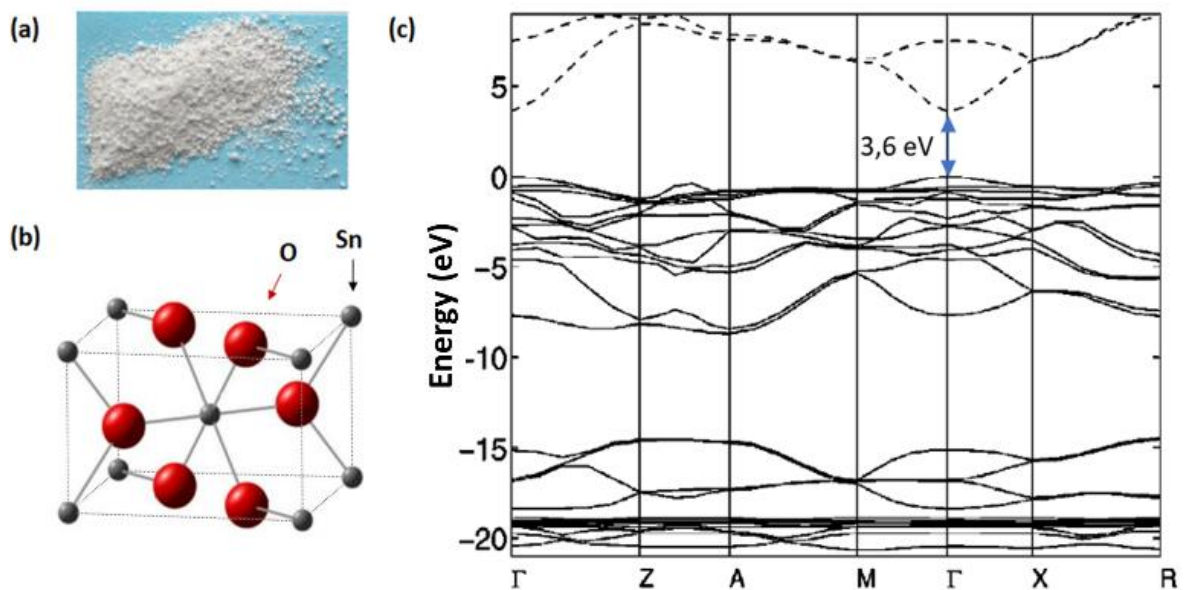
Figure 1 - Tin dioxide's (a) commercial powder, (b) structure and (c) band diagram. Adapted from Ref. [20,21], respectively.

The band diagram calculated using Density Functional Theory (DFT) [20], represented in Figure 1 (c), shows its direct gap of energy, with minimum of the conduction band (CB) and maximum of the valence (VB) located at the Γ (gamma) high symmetry point. The minimum of CB is non-degenerated and formed by Tin's 5s orbitals whereas the maximum of VB is formed by Oxygen's 2p orbitals. It is characterized by a wide band gap of about 3.6 eV, with absorption in the UV region and 97% transparency in the visible region [22], which is the expected behavior for semiconductor metal oxides.

Besides its semiconducting characteristics given by the resistance vs. temperature curve, it is also commonly classified as an intrinsic n-type semiconductor. It is well known that the conductivity in semiconductors can arise from different mechanisms, mainly by thermal excitation, lattice defects, impurities and non-stoichiometry [23]. In SnO_2's case, some of those features combined enable the coexistence of conductivity and transparency in the visible region [22] and the control over its electrical characteristics. For instance, due to non-stoichiometry, defects such as oxygen vacancies can act as shallow donor levels (near the CB) that modify the conductance [24] and also induce absorption only in the infrared region, leading to transparency in the visible range of the spectrum [15,21]. Thus, even without intentional dopant elements, it is possible to control its properties such as the electric resistance (variation between 10^{-2} and 10^{9} ohm.cm [24,25]) through the synthesis, for example.

The construction and study of gas sensors using SnO_2 in the form of film or powder [26] demonstrated its huge feasibility as a sensitive layer. When the dimensions are reduced, numerous advantages compared to its analog in 3D arise [27]. In this condition, such as in nanowires (NW), the surface-volume ratio becomes large, making those defects previously mentioned essential for interactions with the environment in which they are subjected. For instance, current conduction in NWs is sensitive to several external physical agents, such as variation of surface charge by adsorption of gases or optical excitation, in addition to the transport properties resulting from the low dimensionality of the channel [5]. This high sensitivity to changes in the properties of electronic transport and rapid response time contribute to making it possible to detect low concentrations of a chemical component within a short period of time [9,27]. Another feature that stands out in tin dioxide structures, is the wide range of operation related to physiological solutions, which ranges from pH 3 to 10, extending their application as biochemical detectors.

2.2. Metal-Semiconductor Junction

To study devices based on a Metal-Semiconductor-Metal (MSM) structure, it is indispensable to study the Metal-Semiconductor Junction theory, i.e., the Schottky barrier model. The initial theory dates from the end of the 19th century, however, it was only by the late 1930's that W. Schottky, from whom the theory takes its name, assembled a theory that is acceptable up to date. The Schottky barrier model describes the behavior expected for when a metal makes contact with a semiconductor, giving rise to a potential barrier at the metal-semiconductor interface. Such barriers control the current conduction and capacitance [28] and can be studied by energy-band diagrams.

The energy band diagram in this section will take into account an n-type semiconductor and a system without surface states and other deviations. The parameters to describe it are: the Fermi level energy (E_F) of the metal and the semiconductor; the metal's work function (ϕ_m); the semiconductor's electron affinity (χ), conduction band energy (E_C) and valence band energy (E_V); the potential barrier height (ϕ_{Bn}) and the depletion layer (W). As means to understand what happens when a metal makes contact with a semiconductor it is wise to analyze a sequence of four conditions [Figure 2]: (a) metal and semiconductor, electrically neutral and separated from each other; (b) connecting both with a distance δ between them; (c) considering δ when it assumes an interatomic order distance value and, finally, (d) when metal-semiconductor are in full contact.
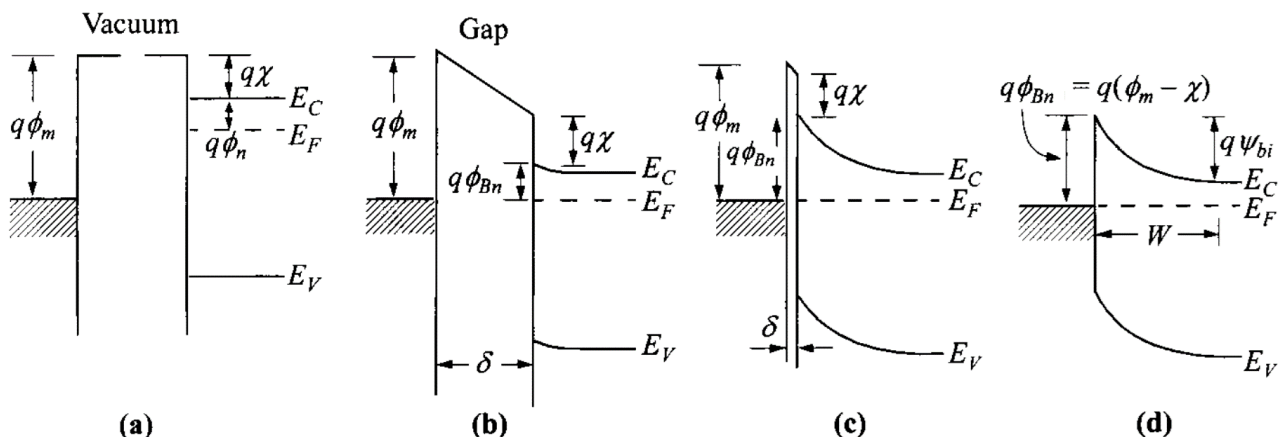
Figure 2 - Energy band diagrams for an ideal junction, when the metal and semiconductor are: (a) apart and neutral, (b) in contact but separated by a layer (δ), (c) when δ → 0 and (d) full contact. Adapted from Ref. [28].

The band diagram depicted in Figure 2 (a) considers a high work-function metal and an n-type semiconductor in separate systems. The work function is defined as the energy difference between the vacuum level and E_F and is equal to $q(\chi + \phi_n)$, in which ϕ_n represents the energy difference between E_C and E_F. A contact potential can be calculated by $q\phi_m - q(\chi + \phi_n)$. The following

situation [Figure 2 (b)], shows the connection between both materials. As a consequence, negative charges are built up on the metal surface and carriers begin to flow from the semiconductor to the metal to reach an equilibrium state. Since the semiconductor has a relatively small carriers' concentration, they tend to distribute in a barrier near the interface. When δ gets small enough, as in Figure 2 (c), the gap between the metal and the semiconductor becomes transparent to electrons, reaching the limiting value of the barrier height $q\phi_{Bn} = q(\phi_m - \chi)$, as shown in Figure 2 (d).

The discussion above is a model for an ideal metal-semiconductor junction. However, in real systems, there is an unavoidable interface layer ($\delta \neq 0$) and the emergence of interface states in the semiconductor [28]. The latter is independent of the metal and can arise from, e.g, irregularities, defects and disorder, which modify the dependence of ϕ_{Bn} on ϕ_m and χ, as suggested by Bardeen [3,29]. Assuming that the disorder in the semiconductor's surface could be represented by a thin oxide layer (δ), it forms an electronic states' distribution on the metal-semiconductor's interface, which are commonly distributed within the band gap energy (E_G).
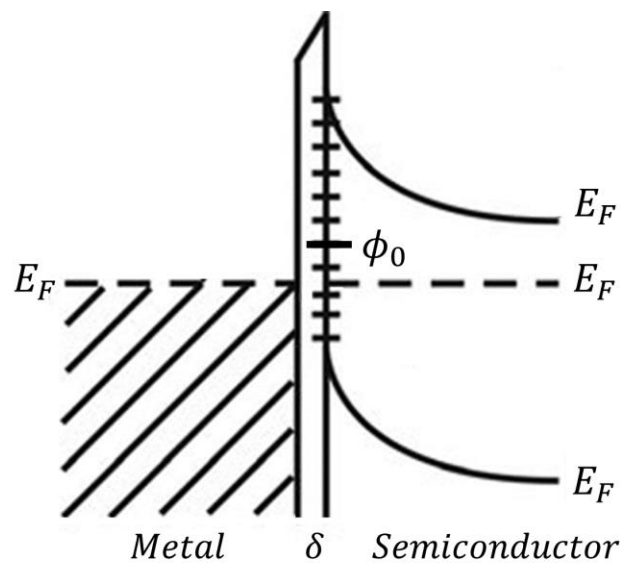
Figure 3 – A metal-semiconductor junction model considering interface states. Adapted from Ref. [28].

As Figure 3 depicts, the states' distribution is characterized by a neutral level ϕ_0 and controls E_F (which is constant throughout the barrier region). For instance, if ϕ_0 is above E_F there is a positive net charge to be taken into account, that consequently diminishes the depletion layer width. Thus, according to ϕ_0 and E_F relation, the depletion layer width and barrier height can be modified, raising or lowering the positive carriers induced in the interface. Given that, it was demonstrated by the Bardeen model that the barrier height is highly independent of the metal [25], and may be

approximated by $\phi_{Bn} = E_G - \phi_0$, indicating that the barrier height is dependent on the presence of interface states [30].

2.3. Field-Effect Transistor (FET)

Among many technological advances throughout the twentieth century, the transistor's invention could be considered as the most important one, since it brought up the necessary tools to innovate the electronics' scenario. Before transistors, vacuum tubes composed electronic systems and performed functions such as signal amplification and current rectification, however, their power consumption was huge and required high maintenance, driving the research for a substitute. By the end of 1947, John Bardeen, Walter Brattain and William Shockley were the three physicists responsible for demonstrating the transistor effect at Bell Laboratories and awarded with the 1956 Nobel Prize in Physics [31] for this achievement. As replacer of the vacuum tubes, they are used as amplifiers, switching circuits, oscillators and in almost all electronic circuits since then [1].

A transistor is generally defined as a three-terminal device whose resistance between two terminals (source/drain) is controlled by the third (gate) [28]. Nowadays, one can categorize a transistor in two types: Potential Effect Transistor (PET) or Field Effect Transistor (FET). Two junctions of different semiconductor types, n-type and p-type, compose the PETs' structures, for instance, a Bipolar Junction Transistor (BJT), whereas a single type composes the FETs and, the devices belonging to this class, are divided according to how the gate capacitor is formed. Junction FETs (JFET) and Metal-Oxide-Semiconductor FETs (MOSFET) structures are the most popular examples, but the latter stands out as the most important component of high-density integrated circuits [28]. The devices in this work were built based on a MOSFET structure, thus it is essential to understand its characteristics.

A typical MOSFET model, represented in Figure 4 (a), is composed by a p-type Silicon substrate which contains an insulating oxide layer (SiO_2) thermally grown on its surface. Two n-type regions are diffused into the substrate and connected by metallic electrical contacts as source and drain terminals while the gate capacitor is formed by a metal in contact with the oxide layer. A conduction channel arises under specific conditions [Figure 4 (c)], dependent on the voltages applied between the source and drain (V_{DS}) and the gate (V_G).
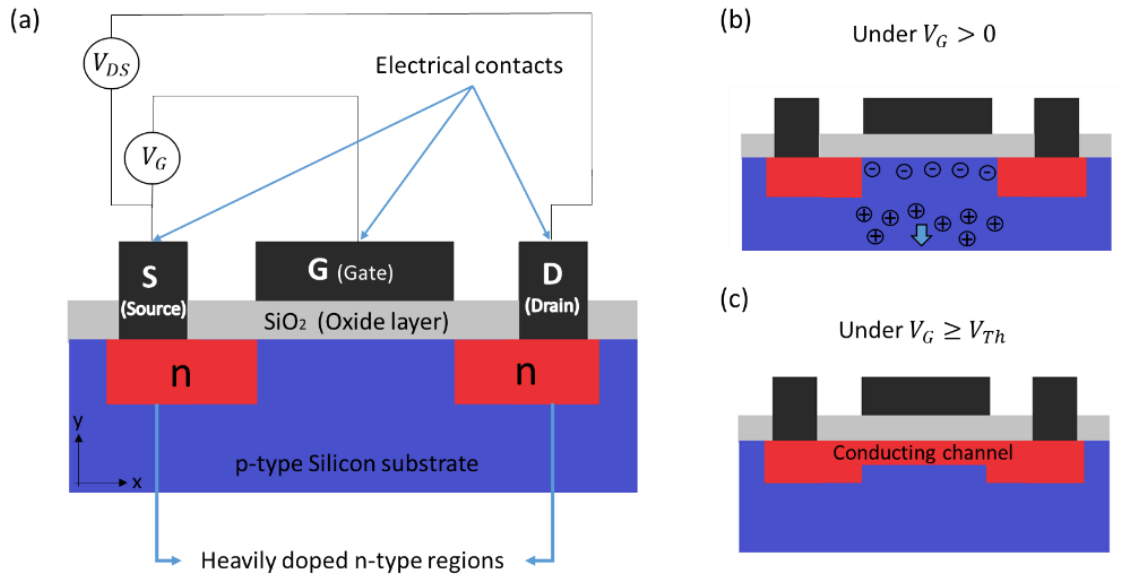
Figure 4 – (a) MOSFET device's representation and its operation in different conditions: (b) under $V_G > 0$ and $V_G \geq V_{Th}$.

As mentioned above, the operating conditions' dependence of the voltages leads to the following possible situations: (1) no voltage applied in both V_{DS} and V_G results in a back-to-back diode configuration; (2) maintaining $V_G = 0$ and setting $V_{DS} > 0$, culminates in two p-n junctions under reverse bias, where no conduction channel is formed; (3) for $V_{DS} = 0$ while gradually increasing V_G, the substrate's majority carriers (holes) start getting depleted, increasing the minority carriers (electrons) availability near the surface [Figure 4 (b)]. When a threshold voltage (V_{Th}) is achieved on the gate, a conducting channel is then formed, as depicted in Figure 4 (c); (4) after the conducting channel is formed, its behavior is dependent on the applied V_{DS} and described by the current-voltage (I-V) characteristics. Figure 5 depicts the band diagrams regarding the MOS interface in the third [Figure 5 (a)] and the fourth [Figure 5 (b)] conditions.
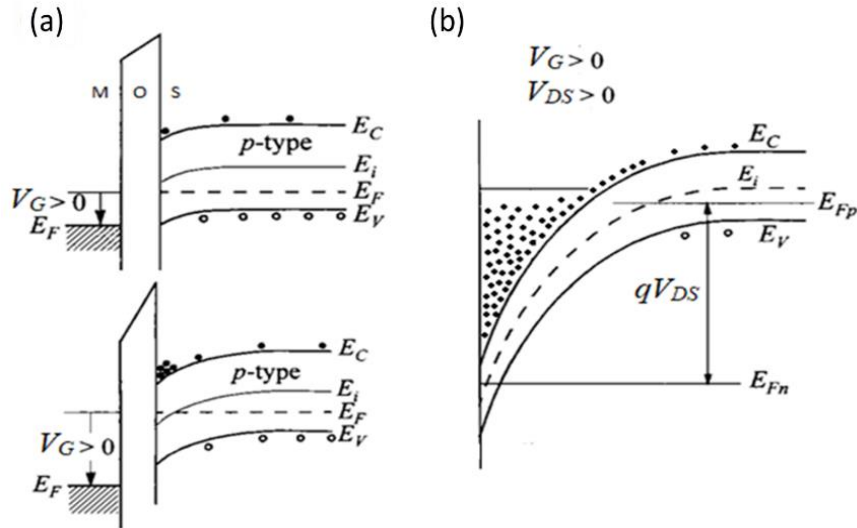
Figure 5- Energy band variation of an inverted p-region from (a) equilibrium to (b) a nonequilibrium state at the drain end. Adapted from Ref. [28].

The idealized I-V characteristics of an n-channel enhancement-mode MOSFET are displayed in Figure 6. The transfer characteristic ($I_D \ vs. V_G$) [Figure 6 (a)] presents the relationship between the conduction and V_{Th}.
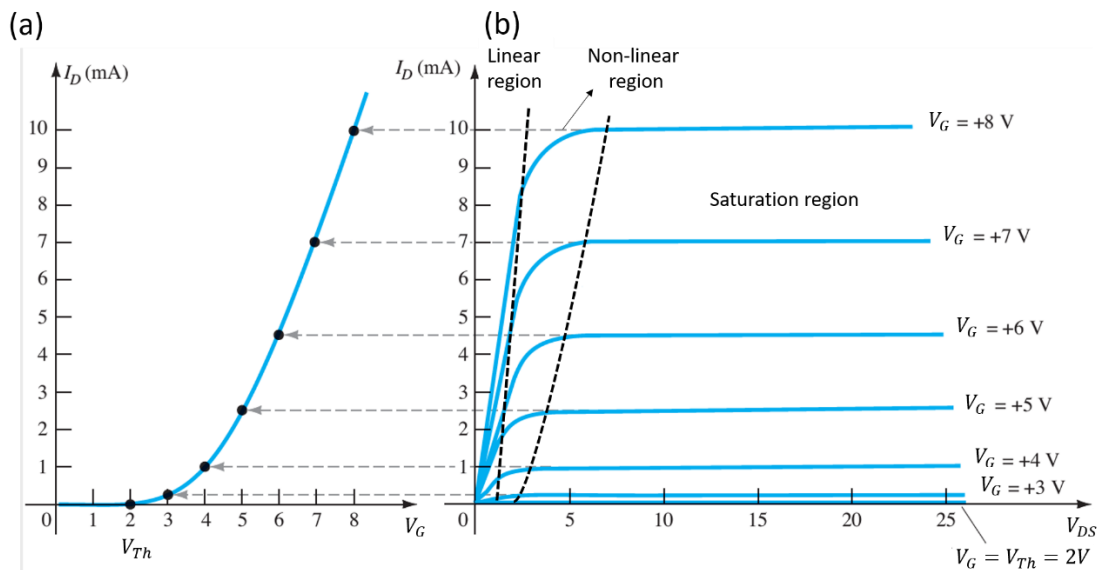
Figure 6 – An n-channel enhancement mode MOSFET and its (a) transfer and (b) output characteristics. Adapted from Ref. [32].

Figure 6 (b) depicts the output characteristic ($I_D \ vs. V_{DS}$), where one can notice three different regions: linear, non-linear and saturation. When a small voltage (V_{DS}) is applied, the channel acts as a resistor and I_D is proportional to V_{DS}, resulting in a linear behavior. As V_{DS} increases and reaches V_G value, the linear relationship is gradually undone (non-linear region) due to charge reduction near the drain end by the channel potential and consequent channel resistance increase. When $V_{DS} =$

$V_G - V_{Th}$, the saturation region is achieved. Two models describe the current equations for those regions: one is the linear model, considering the linear region where V_{DS} is much smaller than $V_G - V_{Th}$ and the other is the quadratic model.

The linear model, as mentioned above, takes into account a small V_{DS} value, so it is described as a linear resistor where its resistance is controlled by V_G. This condition also ensures that the electric field (E), charge (Q_c) and velocity (v) in the channel are constant between the source and drain. The expression for the current in the drain is given by,

$$I_D = \frac{Q_c w L}{t_{tr}},$$ 2.1

where w and L are the channel's width and length, respectively, and t_{tr} the transit time. The transit time is given by $t_{tr} = L/v$ and, within constant electric field and velocity, the field is equal to the applied voltage (V_{DS}) per channel length and the velocity is the product of the mobility (μ) and the field, resulting in

$$I_D = \frac{\mu Q_c V_{DS} w}{L}.$$ 2.2

Associating Q_c with the oxide layer capacitance (C_{ox}) when $V_G > V_{Th}$, it can be written as

$$Q_c = -C_{ox} (V_G - V_{Th}).$$ 2.3

Replacing it in Eq. 2.2, one can find the linear relation between I_D and V_G:

$$I_D = \mu C_{ox} (V_G - V_{Th}) V_{DS}.$$ 2.4

The quadratic model allows one different and important consideration from the linear one, the charge in the channel may vary between source and drain. Also, the current is continuous throughout the channel and it can be related to V_{DS} by

$$I_D = \mu C_{ox} w (V_G - V_{Th} - V(x)) \frac{dV(x)}{dx}.$$ 2.5

Considering an initial voltage V_{DS} and integrating the preceding equation inside the channel length L, one finds

$$I_D = \frac{\mu C_{ox} w}{L} \left[(V_G - V_{Th}) V_{DS} - \frac{(V_{DS})^2}{2} \right].$$ 2.6

In this condition, I_D increases linearly with the applied V_{DS} up to the point it reaches a maximum value, the saturation current. This value for current is achieved when $V_{DS} = V_G - V_{Th}$ and the current equation for the saturation region is given by

$$I_{D,sat} = \frac{\mu C_{ox} W}{2L} (V_G - V_{Th})^2. \qquad 2.7$$

From this model, it is possible to derive the output characteristics and, when transconductance (g_m) is acquired experimentally, it enables to obtain parameters such as the mobility in the channel:

$$g_m = \frac{dI_{D,sat}}{dV_G} = \frac{\mu C_{ox} W}{L} (V_G - V_{Th}). \qquad 2.8$$

The devices in this work were built based on a MOSFET structure, however, differ themselves from it mainly due to the physical existence of a conducting channel, i.e., the NW [Figure 7]. As consequence of this architecture, relations concerning the threshold voltage (V_{th}) and capacitance are modified, leading to a more complex understanding of the device operation [33].
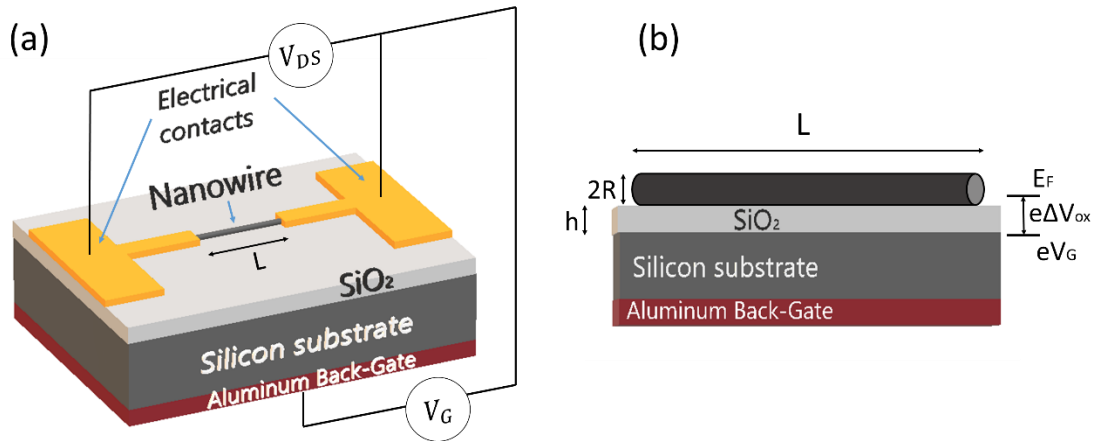
Figure 7 – Representation of a Single NWFET device architecture with: (a) a schematic measurement setup and (b) cross-section representation, in which h is the oxide layer's width, 2R represents the NW's diameter and L its length. Additionally, Fermi energy is represented by E_F, V_{OX} and V_G are the oxide layer's variable potential and gate potential, respectively.

Analogously to the model described for a conventional FET device, a theory concerning a single NWFET and interfaces that arise in its architecture was developed. Instead of a MOS capacitance, the metal-silicon-oxide-nanowire system is considered to calculate the capacitance and it can be described by a known electromagnetism model: the metallic wire placed at a distance h from an infinite metal plate [3], as depicted in Figure 7 (b). However, there is an oxide layer in between resulting in two different capacitances connected in series: the NW and the oxide, C_{NW} and C_{ox},

respectively. Considering the NW radius (r) to be much smaller than the distance to the metal plate ($r \ll h$), the capacitance can be described by:

$$C_{ox} = \frac{2\pi\epsilon_0\epsilon}{ln\left(\frac{2(h+r)}{r}\right)}. \tag{2.9}$$

Such consideration was illustrated by Khanal et al [34] by equipotential analysis of the NW and the oxide (SiO₂) interface. Furthermore, another interface is formed between the NW and air, therefore, two different dielectric constants ($\epsilon_{SiO_2} \approx 3.9$ and $\epsilon_{air} \approx 1$) must be considered. This can be done by taking an effective dielectric constant value $\epsilon_r^{eff}/2\sim2$, where $\epsilon_r^{eff} = \epsilon_{SiO_2} + \epsilon_{air}$.

Likewise, to calculate carriers' mobility related to the device's geometry it is necessary to consider some aspects. The mobility of carriers (μ) within the NW can be calculated when the applied V_{DS} is small enough to assume a uniform potential throughout the channel, i.e., the condition in which $eV_{DS} \ll k_BT \approx 25\ meV$. In such case, the conductance (G_{NW}) for diffuse transport is given by

$$G_{NW} = e\frac{n\mu}{L}, \tag{2.10}$$

in which e is the electron charge, L is the channel length and n is the number of carriers. The latter is described, in terms of the Fermi level energy (E_F), by the density of states $N(E_F)$ and the Fermi-Dirac distribution $f(E_F)$ as follows

$$n(E_F) = \int N(E_F)f(E_F)dE. \tag{2.11}$$

Even though the device's total resistance is characterized by a sum of the channel ($1/G_{NW}$), contact (R_C) and quantum's ($h/4e^2$) resistances, when considering the linear region, i.e., the conditions for Eq. 2.10, only the channel's resistance significantly contributes, since the conductance (G) is dominated by the channel's conductance. Given that, it is possible to calculate the slope by

$$\frac{dG}{dV_G} = \frac{e\mu}{L}\frac{dn}{dE_F}\frac{dE_F}{dV_G}. \tag{2.12}$$

From Figure 7 (b), one can derive dn/dE_F term and the potential drop within the oxide can be expressed as a difference between the gate bias and the NW's Fermi energy, as follows

$$V_G - \frac{E_F}{e} = \Delta V_{ox} = \frac{Q_{ind}}{C_{ox}}, \tag{2.13}$$

where ΔV_{ox} is the variable potential inside the oxide and the channel's induced charge is represented by Q_{ind}. Taking the derivative of V_G [Eq. 2.13] with respect to E_F, rewriting one term as the NWs' quantum capacitance $\left(C_{NW} = e\, {dQ_{ind}}/{dE_F}\right)$ and considering that Fermi-Dirac's distribution becomes a step function with respect to E_F, so ${dn}/{dE_F} = N(E_F)$, Eq. 2.12 can be rewritten as

$$\frac{dG}{dV_G} = \frac{e^2\mu}{L} N(E_F)\left(1 + \frac{C_{NW}}{C_{ox}}\right)^{-1}.$$
2.14

In addition, C_{NW} can be expressed as $e^2 N(E_F)$ and when considering $C_{ox} \ll C_{NW}$, it results in

$$\frac{dG}{dV_G} = \frac{\mu}{L^2}\frac{C_{ox} \cdot C_{NW}}{C_{ox} + C_{NW}} \sim \mu \frac{C_{ox}}{L^2}.$$
2.15

Thus, in the linear regime, expressing the conductance in terms of the current throughout the channel (I_{DS}) with a constant V_{DS} applied, one can obtain

$$\frac{dI_{DS}}{dV_G} \sim \mu \frac{C_{ox}}{L^2} V_{DS},$$
2.16

which is a direct way to relate the $G(V_G)$ slope to the mobility and the device's geometric parameters.

As previously discussed, an n-type semiconductor FET device, e.g., the SnO₂ NWFET, has a typical rectifying response for negative applied V_{DS} voltage, which can be understood as a unipolar mode of operation. Summarizing, when a threshold voltage (V_{th}) is applied on the gate with positive source/drain bias ($V_{DS} > 0$), majority carriers (electrons) are responsible for the conduction, leading to a FET's on state. In $V_{DS} < 0$ condition, the minority carriers (holes) are not enough to provoke the same behavior and conduction is ceased, resulting in a FET's off state. However, an ambipolar mode of operation may arise under specific conditions.

Ambipolarity can be understood as the operation condition in which both types of carriers can contribute to the current. This effect is commonly induced by, for example, dopants, electrical contacts modification and radiation exposure [35-37]. When induced by dopants, the extra carriers intentionally added to the structure can respond to the different bias condition. For instance, if acceptor impurities are added to an n-type semiconductor, electrons are still responsible for the conduction as they were in FET's on state, however, the FET's off state becomes comparable to the on state, since there are enough holes to contribute to the conduction as well [35]. As was described in the previous section, electrical contacts can modify the n-type semiconductor's barrier height ϕ_{Bn},

thus, it is feasible to build a device that can respond to both carriers by choosing suitable materials for the metal-semiconductor junctions, i.e., modifying the Schottky barrier [36]. Ambipolarity effect induced by radiation exposure can be noted in cases where the device is irradiated by a light source with energy equal or higher than the semiconductors' bandgap energy [37]. In such situation, the electron-hole pairs generated by light are dissociated and both carriers can contribute to the current. For instance, a photoconductivity effect arises and increases the electrons' current that already existed, whereas the generated density of holes are sufficient to respond as well. The photoconductivity effect will be explored in the next section.
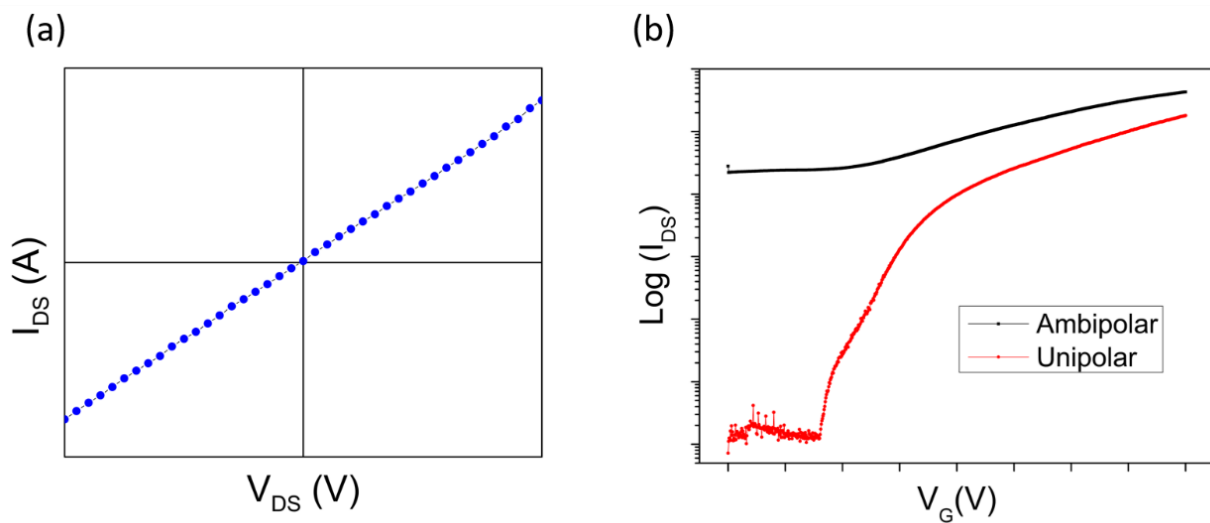
Figure 8 - Examples of ambipolar device's response: (a) output characteristic and (b) transfer characteristics for unipolar (red) and ambipolar (black) operation modes.

Figure 8 depicts examples of ambipolar device's responses. In Figure 8 (a), one can see the output characteristic (I_{DS} $vs.$ V_{DS}), where both carriers contribute so current flows both ways. The transfer characteristics [Figure 8 (b)], are displayed as $\log(I_{DS})$ $vs.$ V_G, for the condition in which there is a huge distinction between on and off states (unipolar mode, in red) and the ambipolar effect, in black, in which on and off states are comparable.

2.4. Photoconductivity

Photoconductivity is a well-known optical and electrical phenomenon in semiconductors [38] and it is one of the processes that leads to photocurrent's emergence. In general, photocurrent is any process where the absorption of photons in materials generates electrical currents. However, when it comes to photoconductivity, the effect is attributed to the separation of photoexcited electron-hole (e-h) pairs by an external electric field [39], which then contribute to the electric current.

The conductivity in a semiconductor is given by the relation between the electrons and holes' concentration $- n$ and p, respectively $-$ and their mobilities (μ_n and μ_p):

$$\sigma = e\mu_n n + e\mu_p p, \qquad\qquad 2.17$$

where e is the electron charge. The extra carriers' contribution to conductivity can be derived from Eq. 2.17, representing the excessive electrons and holes by Δn and Δp. Since they are created simultaneously, there is an equal number of extra electrons and holes, i.e., $\Delta n = \Delta p$. Given that, the photoconductivity contribution to the conductivity can be written as follows

$$\Delta\sigma = e(\mu_n + \mu_p)\Delta n. \qquad\qquad 2.18$$

For this phenomena to take place, the energy of the photons $-$ from a light source, for example $-$ must be equal or larger than the material's bandgap energy. When this condition is satisfied, a sequence of events are likely to happen as depicted in Figure 9: (a) the e-h pair generation and its relaxation to the bottom and top of the conduction and valence band, respectively; (b) e-h pair's recombination and consequent photon emission; and states within the semiconductor's bandgap that can trap carriers (c).
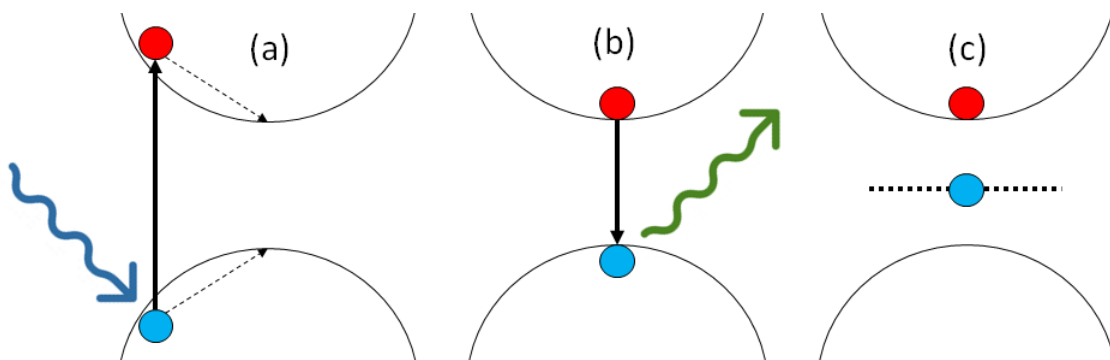
Figure 9 – Schematic diagram of e-h pairs (a) formation, relaxation and (b) recombination. A midgap state is represented in (c), where a carrier can be trapped. Adapted from Ref. [39].

The dashed arrows in Figure 9 (a) represent relaxation processes that the carriers undergo due to scatterings, which is often of the order of femtoseconds [40], until they reach the bottom and top of CB and VB, respectively. The e-h pair's recombination time (τ) can vary from pico to nano seconds [Figure 9 (b)], thus, since photoconductivity is an effect that takes place between the e-h pair's generation until it recombines, it is expected to last for an approximate period of the same order. The photoconductivity gain (G) is dependent on μ_n, τ, the distance between the electrodes (L) and the applied voltage (V):

$$G = \frac{\tau \mu_n V}{L^2}.$$
2.19

This is a discussion regarding an ideal system without any defects. Considering defects or irregularities, states within the semiconductor bandgap may arise and act as traps preventing the pairs from recombining [Figure 9 (c)], which consequently leads to a longer response time of the photoconductivity effect [41]. Experimentally, the photoconductivity characteristics can be studied by recording the current in the dark (off) and in presence of a light source (on), resulting in a response approximately as depicted in Figure 10.
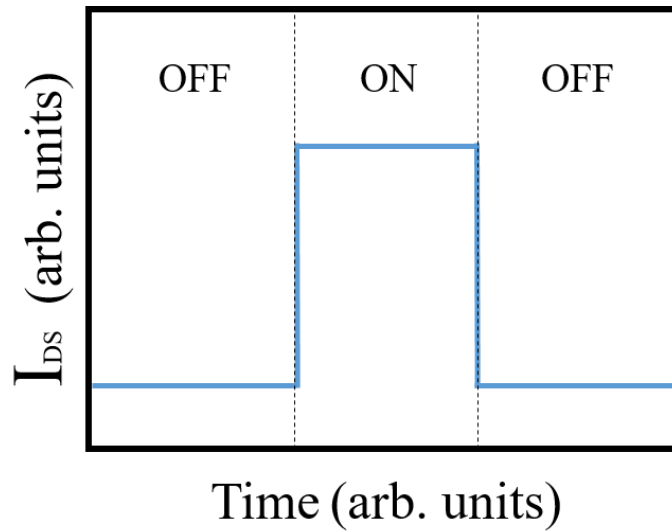
Figure 10 – Photocurrent typical response. Adapted from Ref. [39].

The parameters to be analyzed are: the rise time (τ_r), which is device's response time to the on state condition (when the light source is turned on), and the decay time (τ_d), that can be interpreted as the rapid variation between a state of current saturation and an abrupt drop due to cessation of irradiation [41]. They can be obtained from experimental data fitting to the following equations:

$$I(t) = I_0 \big(1 - e^{-t/\tau_r} \big)$$
2.20

$$I(t) = I_0 + A e^{-t/\tau_d},$$
2.21

where I_0 is the maximum current (steady state), A is a constant and t is the time.

3. Experimental Details

This chapter will present the NW's synthesis chosen method's theory – the Vapor-Liquid-Solid growth mechanism – and discuss parameters that should be taken into account to achieve successful results. Then, an experimental procedure topic will detail the synthesis process of this work's samples, from choosing the substrate and metal catalyst, synthesis parameters and the equipment used to obtain the as-grown NWs. A topic concerning the processes to fabricate a single NW back-gated FET device will discuss some techniques used to obtain the back-gated architecture and electrical contacts by direct recording photolithography technique. At last, the final topic will discuss the techniques used for structural, morphological and electrical characterization of the devices.

3.1. Nanowire's synthesis

Semiconductor nanowire fabrication follows up two distinct approaches: top-down and bottom-up techniques. The first consists on sculpting a larger material into a nano-scaled one and the latter, of this work's interest, are structures assembled from their elemental components [42]. In synthesis routes categorized as bottom-up, methods based on chemical vapor deposition (CVD) are resourceful in terms of crystalline quality and control over the nanowires' diameter [42]. Among them, the Vapor-Liquid-Solid (VLS) growth mechanism stands out as the oldest, most reliable and most studied one.

Vapor-Liquid-solid

The VLS method was originally reported by Wagner and Ellis of Bell Labs in 1964, for Silicon whiskers crystal growth [43]. However, its feasibility on a nanometric scale was demonstrated only by the 90s [44,45]. As the name suggests, this mechanism involves three different phases: it is assisted by metal catalyst nanoparticles (in liquid form) that act as preferential sites for the adsorption of vapor components, which then leads to a guided one-dimensional growth of structures such as whiskers, rods and wires with controlled dimensions [46-48].

The growth mechanism's main steps involve three well-defined phases [49] depicted in Figure 11. As a usual manner to prepare the substrate for growth, the diagram will consider the metal catalyst as a thin film sputtered or deposited [42]. In the presence of heat, there is a transition between (a) and (b) and liquid catalyst nanoparticles are formed. When carried out to the synthesis region, the precursor elements will be absorbed by the nanoparticles forming the first phase: a liquid alloy with

the metal due to the liquid-vapor interaction. Consequently, the second phase takes place and processes of supersaturation and nucleation give start to crystal growth (c), resulting in an unidirectional growth (d), for as long as the precursor is supplied to the system.
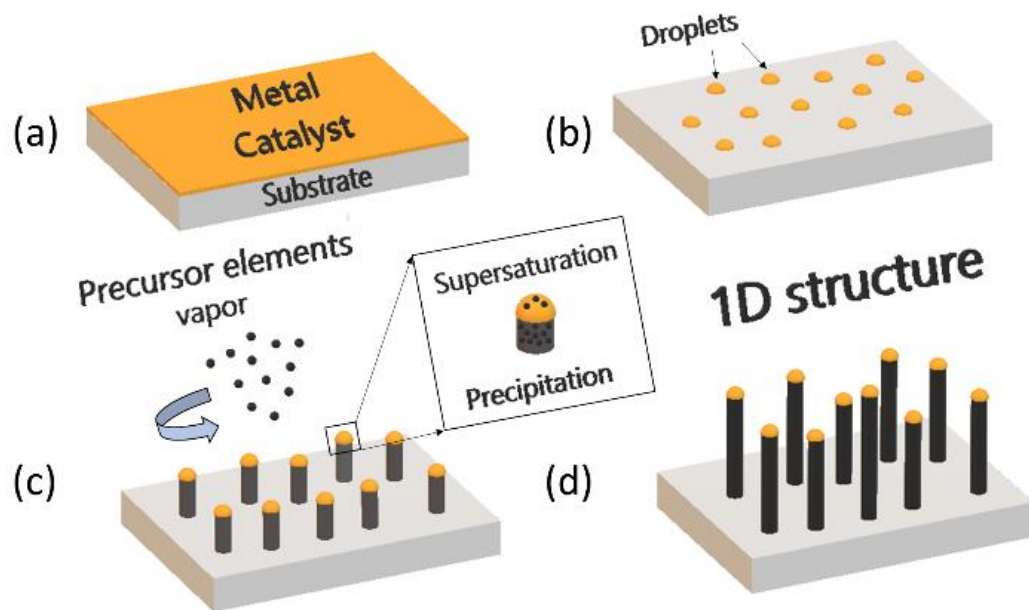
Figure 11 – VLS growth method: (a) Au layer deposition; (b) liquid catalyst nanoparticles formation; (c) process of supersaturation and nucleation that give start to crystal growth, resulting in (d) unidirectional growth. Adapted from Ref. [13].

The metal chosen as a catalyst must have met certain requirements fundamental to the mechanism: it must form a liquid alloy with the precursor; be chemically inert and not make an intermediate solid (or alloy), so it can exercise only its function as a catalytic agent; the vapor pressure of the catalyst over the liquid alloy formed must be small, preventing it from evaporating during the process and the catalyst's solubility in the semiconductor must be much higher in the liquid phase than in the solid one, in order to reduce contamination in the solid phase [13].

As the whole synthesis is a thermodynamic process, a phase diagram is a very useful tool to make the validation of the synthesis parameters, such as the choice of the catalyst, temperature and composition [50]. A binary (A-B) phase diagram is exhibited in Figure 12 (a).
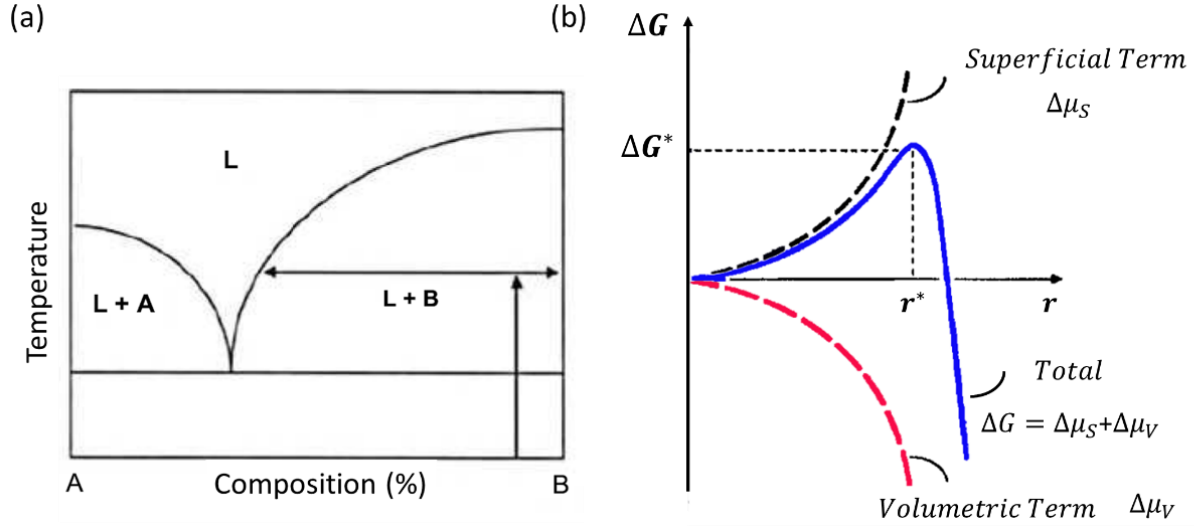
Figure 12 - a) Binary phase diagram Diagram and (b) and illustration of the Gibbs free energy change and the nanoparticle's radius. Above the critical radius, it is thermodynamically favorable for the particles to form and grow. Adapted from Ref. [25].

The vertical arrow in Figure 12 (a) indicates a specific catalyst's composition (A) to a NW (B) and the arrow's end point represents the NW's growth temperature. The horizontal arrow defines the liquid catalyst composition (L) and the NW-catalyst nanoparticle (A-B), in addition it depicts that the solid pure NW (B) is the only solid phase in this temperature [51,52]. Physical processes of nanostructures' growth are described by Gibbs free energy (ΔG), as depicted in Figure 12 (b). As mentioned before, supersaturation of the liquid alloy is the first step towards growth, followed by nucleation. When the liquid alloy achieves a supersaturation point it has a high corresponding ΔG value and the system, in order to reduce it, enables a solid phase to be formed. Gibbs free energy by unit of volume in the solid phase (ΔG_V) is dependent on the solute concentration (C) as follows:

$$\Delta G_V = -\frac{k_B T}{\Omega} \ln \frac{C}{C_0} = -\frac{k_B T}{\Omega} \ln(1 + \sigma),$$ 3.1

where Ω is the atomic volume, C_0 is the solubility (equilibrium concentration) and σ is defined as the supersaturation $[(C - C_0)/C_0]$. Without supersaturation ($\sigma = 0$), ΔG_V is zero and there is no nucleation, whereas if $C > C_0$, ΔG_V is negative and nucleation spontaneously occurs. Considering a spherical nucleus with radius r, the volumetric energy variation ($\Delta \mu_V$) is described by

$$\Delta \mu_V = \frac{4}{3} \pi r^3 \Delta G_V.$$ 3.2

As the new phase arises, also does a superficial energy ($\Delta \mu_S$) to counterbalance the energy reduction, given by

$$\Delta \mu_S = 4\pi r^2 \sigma.$$ 3.3

The total energy variation ($\Delta G(r)$) for nucleus formation is then given by a sum of both parameters ($\Delta G(r) = \Delta\mu_V + \Delta\mu_S$). One can see, in Figure 12 (b), that the nucleus will be stable when it exceeds a critical radius value $r = r^*$. This value can be obtained when $d\Delta G/dr = 0$ and is also used to acquire the nucleation energy's maximum of $\Delta G(r)^*$, i.e., the activation barrier for nucleation. After the initial nucleation process, Gibbs free energy must decrease and supersaturation must increase, in such a way that no new nuclei are formed and NW's growth are favored until solute's concentration achieves solubility, as in the final stage depicted in Figure 12 (b).

3.2. Experimental procedure

Initially, thin films of gold (15Å) were deposited (Edwards 306 coating system) in previously prepared Si/SiO$_2$ substrates (oxide layer 500 nm thick) in order to generate the catalyst nanoparticles. From this point, it was necessary to proceed with optimized Tin dioxide's synthesis parameters, which were provided by extensive studies previously performed by our group [3,5,9,24,25]. The synthesis was carried out in a tube reactor system (Lindberg Blue M), where a high purity Tin powder (0.1 g, Aldrich, purity > 99.99 %) was placed in an alumina crucible which was positioned at the center of the reactor and heated to 950°C (heating rate of 18.5°C/min) and remained at this value for 60 min [Figure 13].
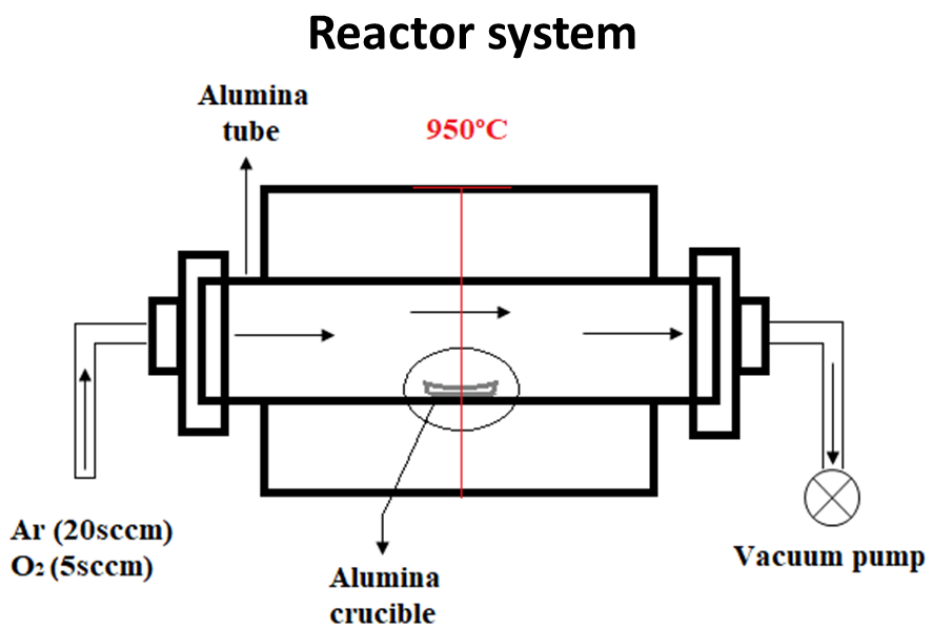
Figure 13 - Side view representation of the used reactor. Adapted from Ref. [13].

For the vapor transport to the synthesis region and as a source of oxygen atoms, an Argon/Oxygen mixture with a constant flow of 20/5 sccm (Mass Flow MKS 1149), respectively, was maintained along

with controlled pressure by a vacuum pump around 350 mbar. Due to the reactor's length, a relatively wide temperature range can be observed throughout the tube, requiring the study of a specific temperature-position distribution diagram for this equipment. Therefore, a well-established temperature-position curve built by NanOLaB's team, depicted in Figure 14, was used to guarantee the temperature stability. One can notice that the temperature is maintained at 950°C in a 20 cm range (between -10 and 10 cm), assuring that this temperature was kept unchanged throughout synthesis.
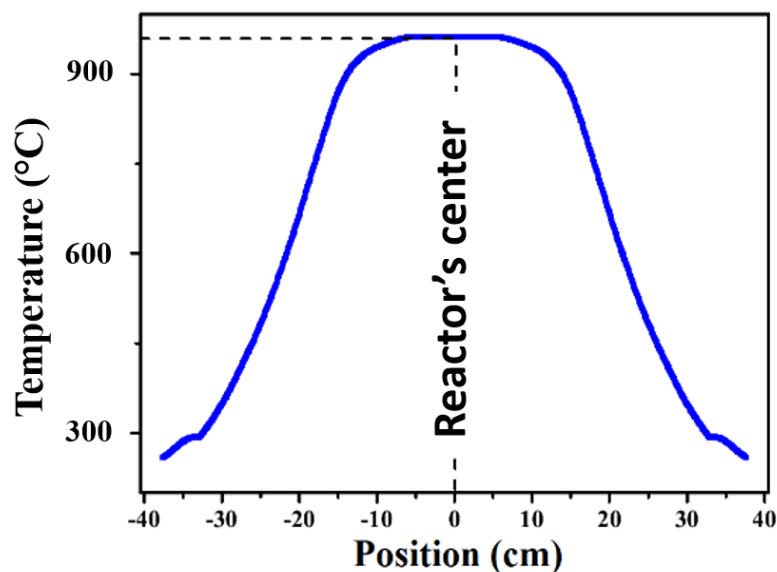
Figure 14 - Diagram illustrating the temperature distribution along the alumina tube inside the reactor. Adapted from Ref. [25]

Figure 15 displays four substrates resulting from this VLS synthesis. In some of them [Figure 15 (a)], one can notice the absence of nanowires where there was no Au deposited, ratifying the VLS growth mechanism. In addition, a scanning electron microscopy (SEM) image was obtained between those two areas as means to highlight this difference [Figure 15 (b)]. From a first analyses of the substrates, it is reasonable to say that a high density of NWs was obtained.
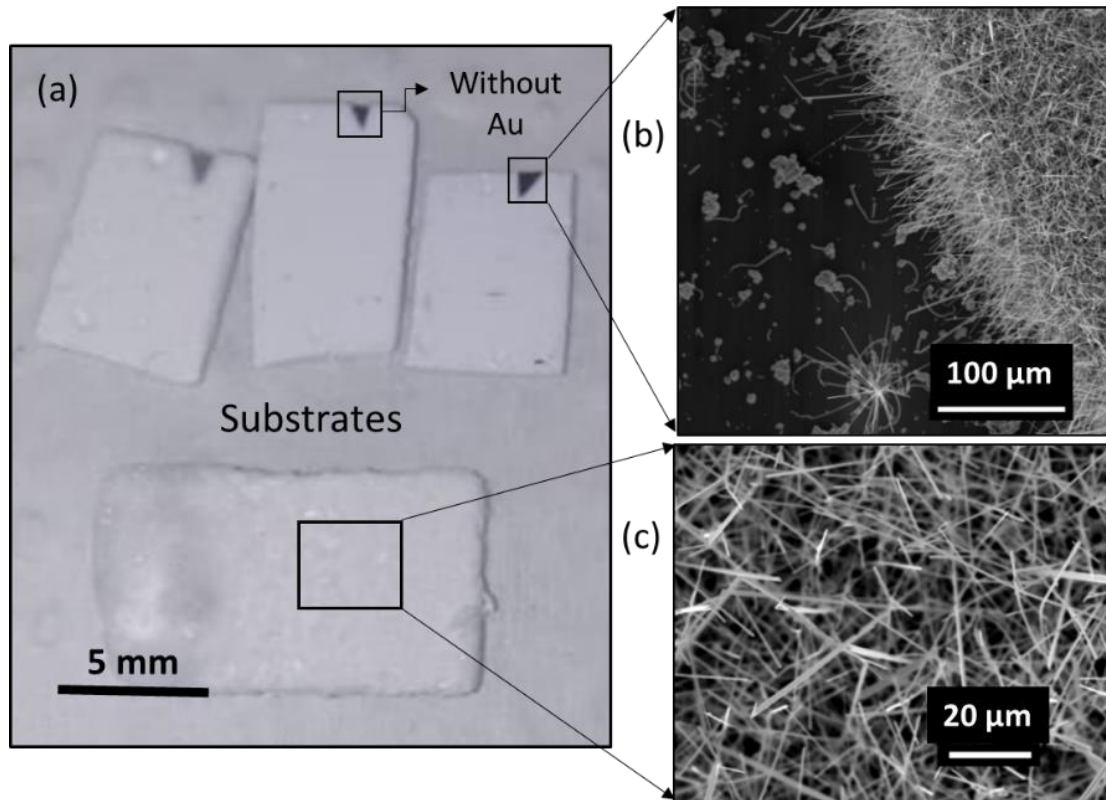
Figure 15 – Synthesis' results from VLS growth of nanowires: (a) image of four different substrates grown under the same conditions; (b) the absence of nanowires where there were no catalyst nanoparticles and (c) a SEM image of the nanowires on the substrate.

Also, Figure 15 (c) presents a SEM image of the NWs network grown on one of the substrates, where the desired structures, NWs, can be seen with diameter and length of tens of nanometers and micrometers, respectively.

3.3. Device fabrication process

The manufactured devices have a back-gate FET architecture; therefore, the first step consisted on a 100nm thickness Aluminum layer deposition (Edwards 306 coating system) on the back of the substrate. In a clean room environment, NWs were dispersed in an ethanol solution by means of ultrasonic stirring for a period of 30 minutes. At this stage, it was essential to wait for the solution to decant, in order to collect the floating material only, which contained the smallest NWs. Using a micropipette, onto previously cleaned substrates 1-3 µL of the prepared solution was dripped. After natural drying, a layer of a photosensitive film (Shipley S1805 photoresist) was deposited on the substrates, using the spin-coating technique with controlled speed and time.

The process chosen to build the device, which contains a single nanowire, was direct recording photolithography (Durham MicroWriter, model ML3 Baby, Scotland), a method to build devices with

no need of a pre-defined pattern mask. The MicroWriter is equipped with a software that, through a system of coordinates, enables to locate a single nanowire and create the desired electrical contact pattern on its surroundings. Instead of a pattern mask, it uses computer-controlled optics to transfer the pattern directly on the photoresist coated substrate. This process is partially represented in Figure 16: one can see the first stages of fabrication in (a) and (b), which involve the NWs and photoresist's deposition. In sequence, the photolithography process (c), when a suitable pattern is transferred to the substrate through UV exposure. Then, the pattern is etched (d), preparing the surface to a metallization process by deposition. The final step, known as lift-off (e), is carried out so the metal remains only in the desired locations. Following those steps, all devices studied in this work were produced.
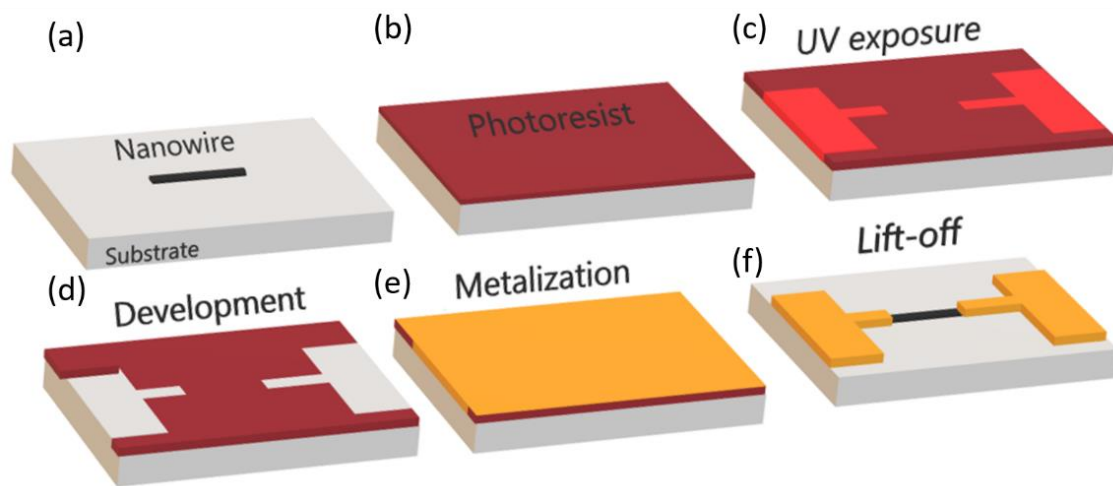
Figure 16 – Step by step of the photolithography process: (a) the chosen nanowire; (b) photoresist's deposition; (c) UV exposure; (d) the development, in which the pattern is prepared for (e) metallization and (f) lift-off.

The devices resulting from those procedures are displayed in Figure 17. The first one, Figure 17 (a), shows a substrate with seven numbered devices, whereas Figure 17 (b) and (c) are optical images of a specific one (device number 6), acquired with an optical microscope (Zeiss imager.M2m, from NanOLaB).
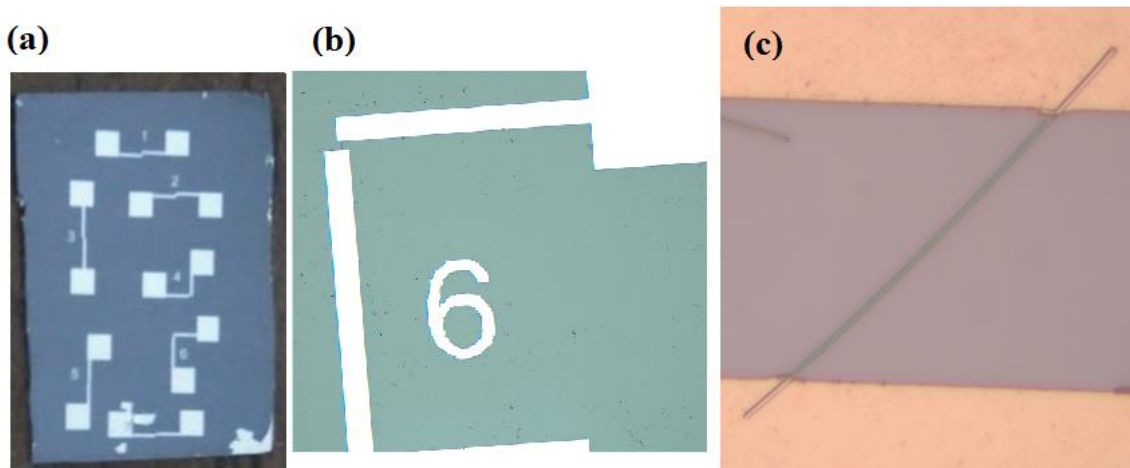
Figure 17 – Devices resulting from the fabrication method presenting: (a) a picture of the whole substrate, and optical microscope images of a chosen device highlighting (b) the electrical contacts and (c) the nanowire.

Figure 17 (c) also displays the NW and two electric contacts deposited at its ends, indicating the device fabrication procedure's high quality.

3.4. Structural characterization

As the first step consists in synthesizing SnO_2 nanowires, it is indispensable to make use of different techniques that verify the synthesis quality and morphology obtained. X-ray diffraction pattern (XRD) technique, Scanning electron microscopy (SEM) and Transmission electron microscopy (TEM) were used in this work for such purposes.

X-ray diffraction pattern: X-ray diffraction is a tool for investigation of a crystal's structure [53]. In this work, it was used as means to assure that tin dioxide's tetragonal structure was obtained. As-synthesized samples were examined by X-ray diffraction Rigaku D/max-2500, Cu-Kα radiation.

Transmission electron microscopy: By illuminating the sample with an electron beam and detecting the electrons that are transmitted through it, one can investigate crystal structures, specimen orientations and chemical compositions of phases. In addition, a High Resolution Transmission Electron Microscopy (HRTEM) enables to see the columns of atoms present in crystalline samples. Such techniques were explored in order to analyze tin dioxide's crystalline structure and verify the result obtained by XRD. An electronic microscope FEI Tecnai G2 F20, from LIEC-DQ/UFSCar, was used to acquire data mentioned above.

Scanning electron microscopy: This technique enables a morphological analysis of a sample. A focused beam of electrons sweeps its surface and provides information concerning its superficial

homogeneity, macroscopic defects and structures formed. A microscope JEOL JSM 6510, from NanO Lab, was used for acquiring images.

3.5. Electrical characterization

For all measurements, an electrometer (Keithley 6517-A) and a source (Keithley 2400) were used as gate and source/drain, respectively, as depicted in Figure 18.
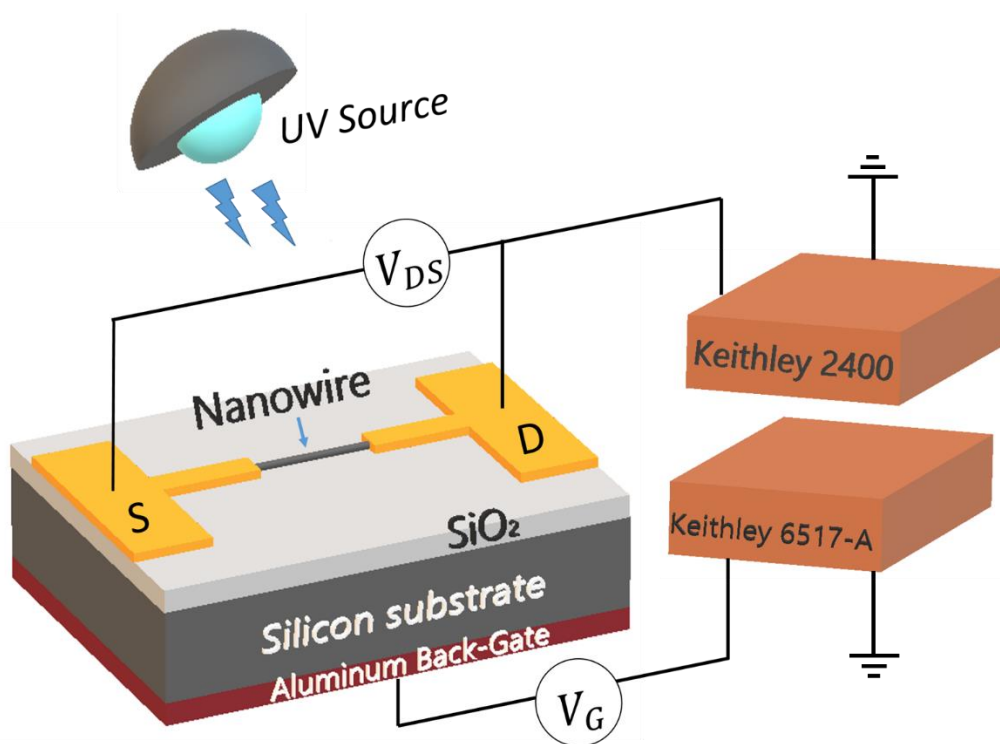
Figure 18 - Schematic of the electrical characterization setup with a UV source.

When containing light excitation source, a UV Lamp (Cole-Parmer UVGL-15 - 2 mW/cm^2) with main spectral lines at 254 and 365 nm was used and a chopper to generate the on and off states. To verify the reproducibility of the devices, a total of seven samples grown under the same synthesis conditions and built in the same architecture were analyzed.

4. Results and Discussion

This chapter will present all the results regarding (1) the basic properties of the synthesized samples such as structural and morphological ones obtained from XRD, SEM and MEV data analysis as well as (2) devices' electric operational parameters. As already described, after these basic characterization, samples were used to assemble different electrical devices. These devices went through different electrical characterizations to obtain parameters related to transistors' basic responses, such as output and transference characteristics, for dark and under UV illumination conditions. Those measurements enabled to acquire mobility and carrier density parameters and, besides that, when under UV illumination the samples presented an ambipolar effect. A simple band model will discuss the origin of this effect. Furthermore, a final topic will explore the use of such devices as UV photodetectors.

4.1. Structure and morphology

As means to examine the NW's structure and morphology, XRD pattern and TEM images were used as tools, respectively. Figure 19 depicts the XRD of as-grown samples. All indexed diffraction peaks show rutile-like peaks (JCPDS 41–1445) [54] as expected for the tetragonal structure of SnO_2 (a = 4.738Å and c = 3.187Å) within the $P4_2/mnm$ spatial group.
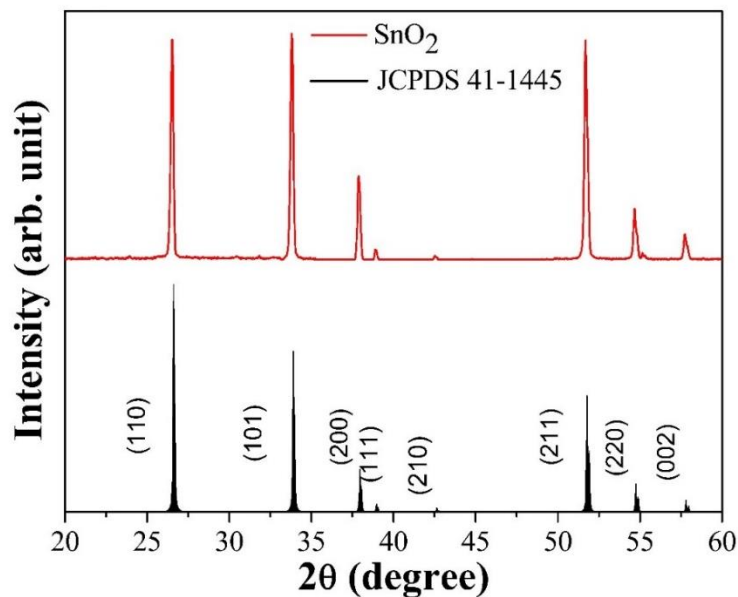
Figure 19 – XRD pattern of the as-grown samples (red) displaying the rutile like peaks (JCPDS 41-1445, black).

Through TEM image and its fast-Fourier transform, the morphology was analyzed and the XRD results previously acquired were ratified as follows. Figure 20 (a) displays a TEM image of a single NW, presenting the desired morphology for this work. The selected region, Figure 20 (b), shows a HRTEM image indicating that the nanowires are monocrystalline and confirming the sample's high crystalline quality. Figure 20 (c) presents the respective Laue pattern, depicting two sets of planes with spacing of 2.64 Å and 2.36 Å, corresponding to (101) and (200) planes, respectively.
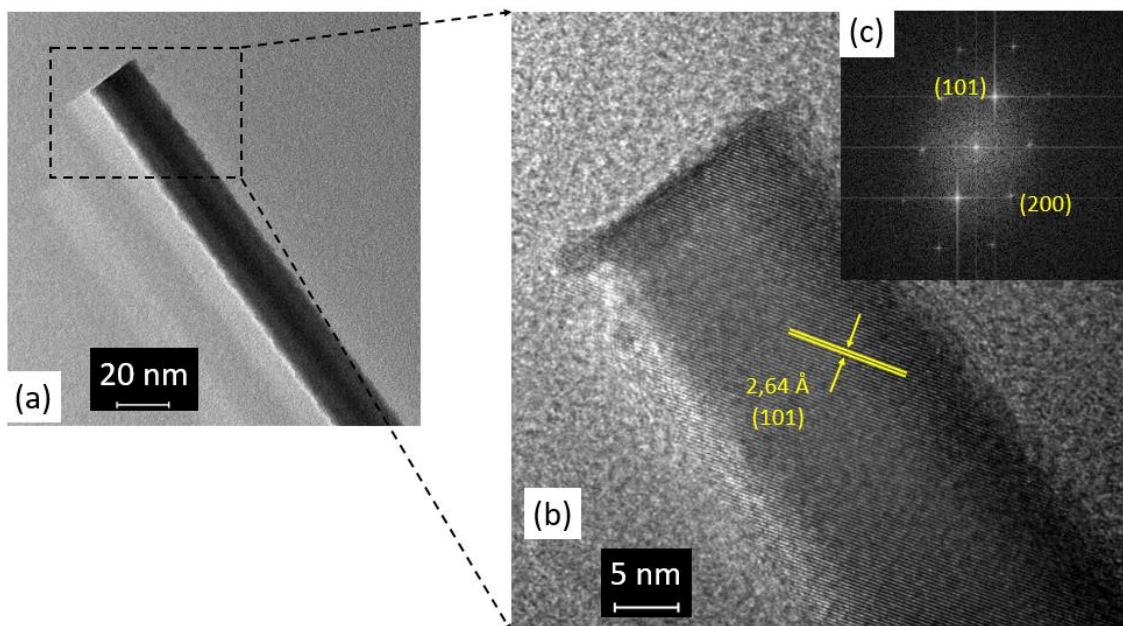
Figure 20 - Exhibits a SnO2 NW's: (a) TEM image, (b) HRTEM and its fast-Fourier transform in (c). The latter highlights two sets of planes with spacing of 2.64 Å and 2.36 Å, corresponding to (101) and (200) planes of SnO2's rutile phase, respectively.

SEM images of VLS synthesis are presented in Figure 21. One can note structures with lengths of tens of micrometers and cross-section mostly displaying rectangular geometry.
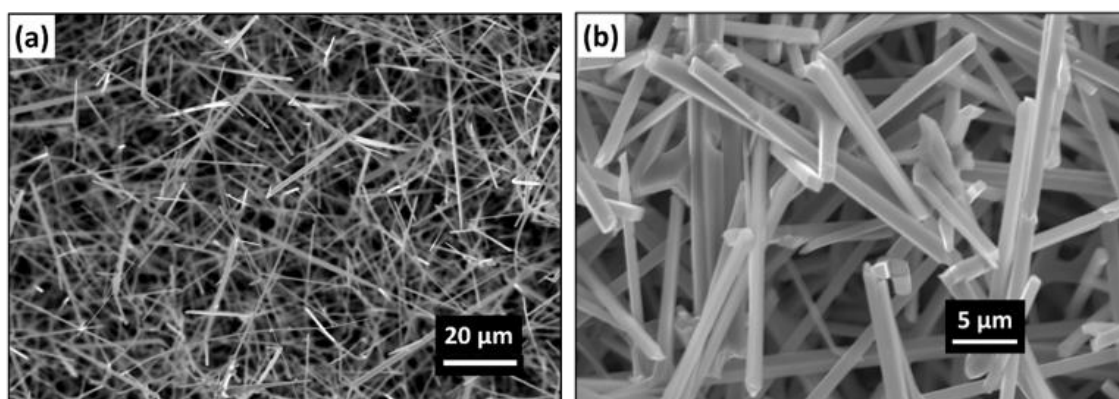
Figure 21 - SEM images of the nanowire network.

Moreover, it is also possible to observe multiple branched nanowires that can arise during the synthesis process of one-dimensional nanostructures, known as self-catalytic dendrites [55], although there is no interference in our results.

4.2. Electrical characterization

In this section, the results regarding $I_{DS} - V_{DS}$ characteristic curves and transistor's fundamental properties with and without UV exposure will be discussed. The analysis' outcome of the UV exposure data revealed an ambipolar mode of operation for all devices under inspection, instigating further investigation. As means to understand such behavior, a simple band model for this effect will be proposed and discussed. In addition, since the devices presented a good response under UV illumination, i.e., a significant increase in the current value, their application as UV photodetectors will be briefly discussed.

4.2.1. SnO$_2$ NWFET's properties and ambipolarity effect

As described in section 3.3, single SnO$_2$ NWFET devices were fabricated with a back-gate architecture and seven of them went through all the analysis that will be shown in here. Firstly, $I_{DS} - V_{DS}$ characteristic curves varying the applied gate voltage are obtained to assure a transistor-like behavior. Figure 22 shows $I_{DS} - V_{DS}$ ($-5\,V < V_{DS} < 5\,V$) characteristic curves for different values of V_G, ranging from -10 to 10 V in step of 2 V under dark and UV exposure conditions. Those measurements were performed in the dark and at room temperature. One can note the expected behavior for an n-type semiconductor: the conduction increases with positive V_G and V_{DS} values and it is almost ceased when otherwise.
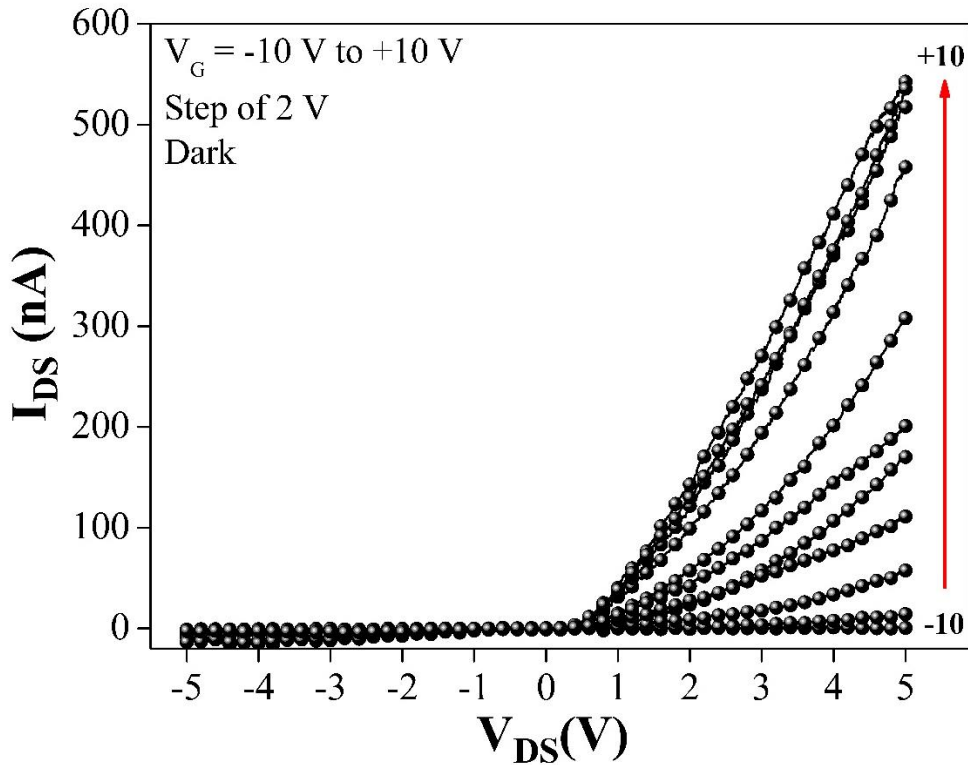
Figure 22 - $I_{DS} - V_{DS}$ curves with different gate applied voltages for dark condition.

Followed by assuring that the devices have a transistor-like response, a UV exposure condition was chosen to inspect the devices' behavior, such as photoconductivity, since the UV light source has higher energy than SnO_2's band gap. It is interesting to mention that light excitation (chosen according to the band gap energy of the studied samples) is widely used in our laboratory to confirm that the device is working correctly and that the electrical signals come from the active region, in other words, from NWs. Since the substrates used to build the devices (and problems like unavoidable conduction paths created by remnants of the assembly process) do not have any photoresponse under the light excitation used here, this procedure ensures that the devices are properly working.

Figure 23 presents $I_{DS} - V_{DS}$ curves for both conditions, dark (black) and illuminated (blue), both under $V_{DS} = \pm 5\ V$ and V_G grounded: the photoinduced behavior is readily observed with an expressive increase of the I_{DS} current. From this result, it was possible to recognize clearly the photoconductivity effect for positive V_{DS} values; however, a similar behavior was also noticed when negative V_{DS} values were applied.
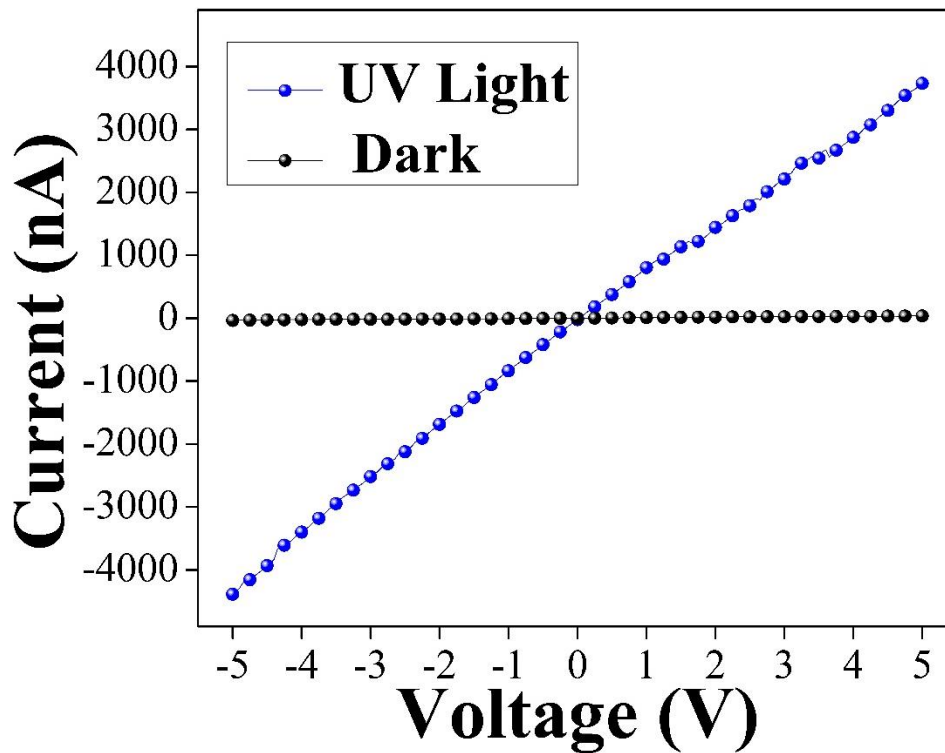
Figure 23 - $I_{DS} - V_{DS}$ curves, with the gate bias grounded, for the dark condition (black) and under UV Light (blue).

To initiate the discussion, the photoconductivity effect in TCOs, such as SnO_2, must be understood. Thus, some important mechanisms and their relationship will be discussed as follows. Basically, all studies conducted in metal-oxide nanostructures carried out to date point out the electronic transport as deeply dependent on the role played by oxygen vacancies. For a single nanowire, surface effects related to oxygen adsorption/desorption and the electron-hole pair dissociation due to the applied voltage take place simultaneously [4]. In the first case, oxygen molecules are adsorbed on the SnO_2 surface by capturing the electrons (O_2(gas)+ $e^-\rightarrow O^{-2}$(ads.)) and after illumination, some of these photo-generated charges tend to migrate to the nanowire surface to discharge the adsorbed oxygen ion (O^{-2}(ads.)+ $h^+\rightarrow O_2$(gas)), as is shown in Figure 24. In the latter case, there is a conductive channel inside the nanowire and the e–h pair generated due to the absorbed photon is separated by the applied external electric field resulting in an increment of the current caused by additional electrons.
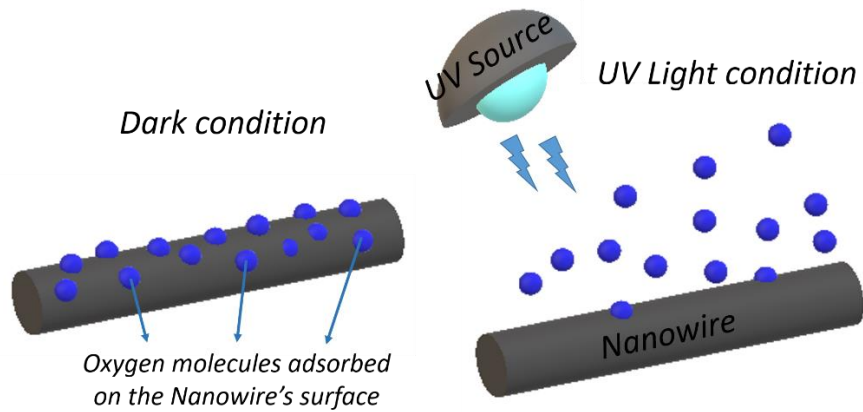
Figure 24 - Schematic of oxygen molecules adsorption on the NW's surface and, when under UV Light, their desorption from the surface.

However, this well-known scenario [4] was not readily observed regarding the FET devices studied here. When negative V_{DS} values were applied, there was also a photoconductivity response, as can be seen in Figure 23. To ascertain that it persists when V_G is not grounded, as it was done for the dark condition, the samples went through inspection for different values of V_G, ranging from -10 to 10 V in step of 2 V, but now under UV illumination. The sets of curves resulting from the UV expose are depicted in Figure 25.
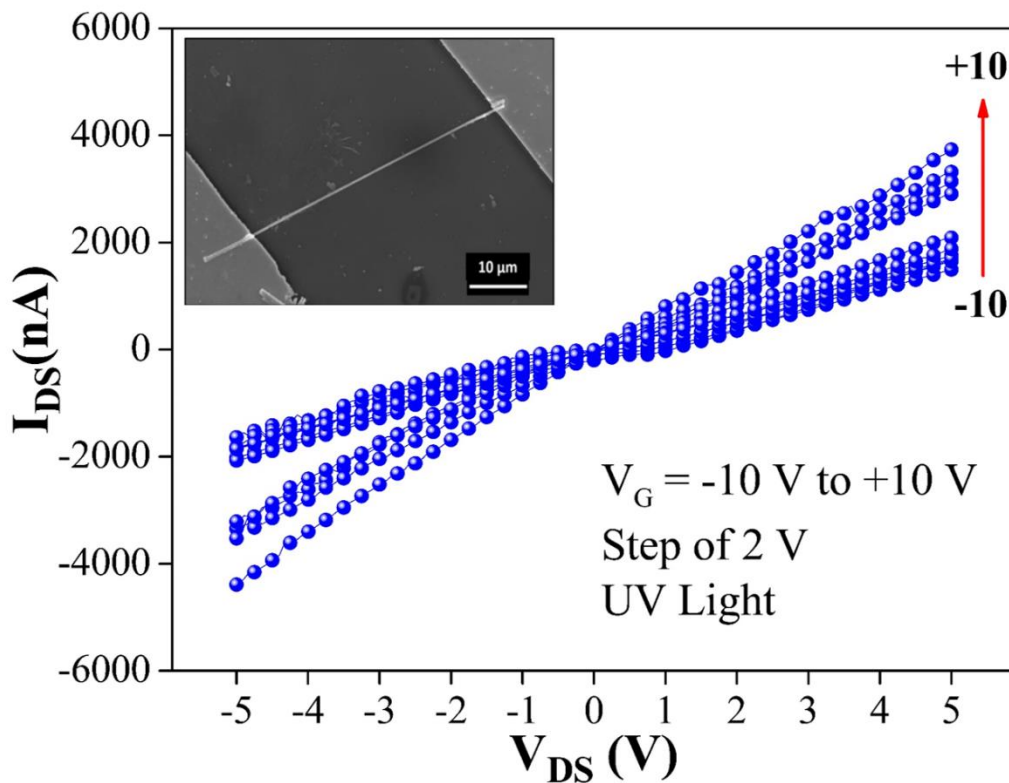
Figure 25 - $I_{DS} - V_{DS}$ curves with different gate applied voltages for UV Light illumination condition. The inset is a SEM image of a single NWFET device studied.

When under UV Light, the behavior noted in Figure 22 is modified resulting in a different set of curves [Figure 25]. The conduction increases in both conditions: when V_G and V_{DS} are both positive and negative. The first one can be attributed to the photoconductivity effect expected as explored before, but the latter reveals an effect of UV induced ambipolarity. Mainly, this effect can be attributed to a not negligible holes density excited by light, however, how does it contribute to the conduction will be further discussed in a proposed model. Before that, some other properties of the devices need to be discussed.

Transistors' fundamental properties were extracted out from their transfer curves ($I_{DS} - V_G$), such as the threshold voltage (V_{th}) displayed in Figure 26 for seven different studied devices, where $V_{DS} = 2\ V$ was considered for all.
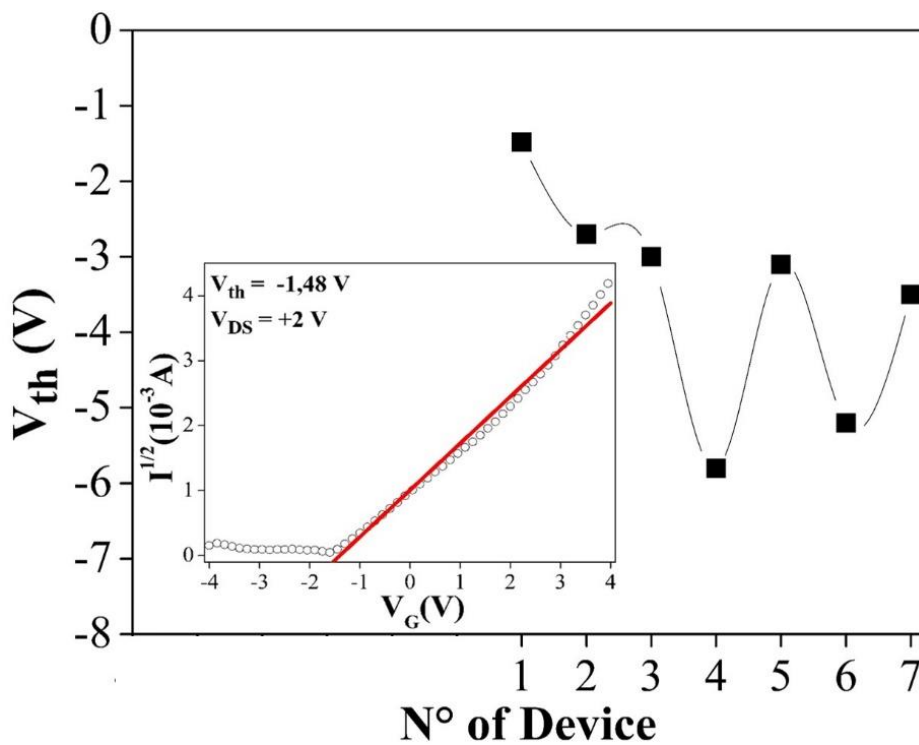
Figure 26 - Threshold voltage values for seven representative devices. Inset depicts a linear fit to obtain such parameter.

Its evaluation is shown in the inset, where a linear fit was used for each $\sqrt{I_{DS}} - V_G$ curve to extract out V_{th} values. This parameter represents the value of voltage applied in V_G that gives rise to a field effect, for the chosen V_{DS} value. The values found for the devices ranged between -5.8 and -1.48 V ($-5.8\ V < V_{th} < -1.48\ V$). The carrier density and mobility of each device could be also obtained using the threshold voltage [Eq. 2.16] as follows. The carrier density (n) and the mobility (μ) are both dependent on the oxide capacitance (C_{ox}), given by Eq. 2.9. The length range was between 39-56 μm

and the diameters from 120 to 680 nm, thus a $C_{OX} \approx 10^{-11} F$ was estimated for the devices used here.

Figure 27 depicts parameters for the seven samples in the dark: the carrier density, calculated by the relation $n = C_{OX} V_{th} / e\pi (d/2)^2 L$, resulting in different values of the same order (10^{19}/cm³) and the mobility, given by $\mu = (dI_D / dV_G) L^2 / C_{OX} V_{DS}$, which resulted in values smaller than 0.1 cm²/Vs. Those values are lower than some reported values [56,57], however are of the same order. Since devices under UV illumination yielded a resistor-like behavior [58], calculating such parameters for holes, i.e., mobility and carrier density, do not lead to reliable results.
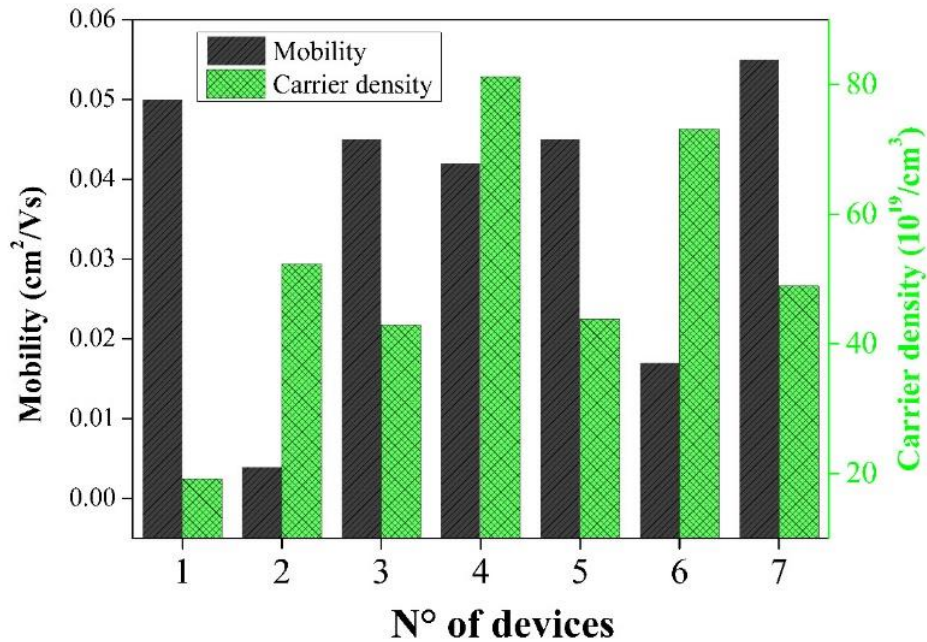
Figure 27 - Mobility (black) and carrier density (green) for the seven studied devices.

Figure 28 displays $Log(I_D) - V_G$ curves for both conditions: in the dark (black) and under UV Light (blue). Usually, to analyze the device's response, a ratio between the on state and the off state is taken. The on-state is related to the region in which there is a field-effect response ($V_{DS} \geq V_{th}$) and the off-state is the one with no significant conduction ($V_{DS} < V_{th}$). When analyzing Figure 28, one can notice that the dark condition curve, in black, presents a high on/off ratio of about 10^5. All seven curves were analyzed and only for one of the devices this value was decreased by one order.
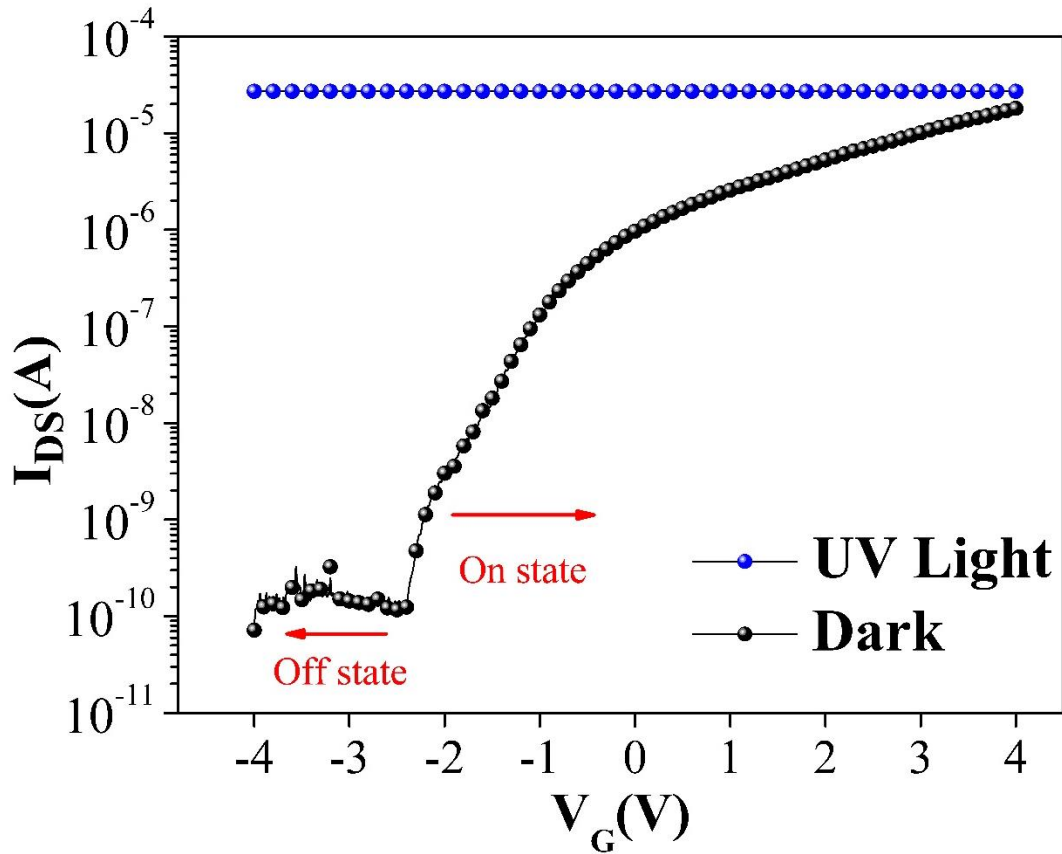
Figure 28 - (b) Transfer curves for the dark (black) and UV exposed (blue) conditions (for a representative device).

The results found for the devices under UV illumination reveal on/off states ratio with values of the same order, ranging from 1.1 to about 19.3. Those results are a consequence of what was already seen in $I_{DS} - V_{DS}$ curves [Figure 25] and indicate that the space charge regions inside the NWs produce a variation of the conductive volume when carriers are photogenerated [59]. Since all samples present similar response, a model is proposed to understand what events take place when the devices are under UV Light.

The model proposed to explain the behavior observed for the dark and illuminated conditions consists in the analyses of different interfaces conditions created by the device's architecture. It should be emphasized the qualitative character of the model: it shows in a simple way that we can observe contribution of both electrons and holes in n-channel FET nanowire device when a non-neglectable holes density is excited by light. The p-type behavior is limited to certain values of gate and source-drain bias and can be explained by positive charge buildup on the metal-semiconductor contacts.

The studied devices are composed by two equal Au/Ni electrodes, in which its average work function's value (Φ_m) may be around 5.1 eV. Ideally, the barrier height (Φ_{Bn}) of an n-type semiconductor can be expressed as $\Phi_m - \chi^{SnO_2}$, with tin dioxide's electron affinity represented by χ^{SnO_2}. The latter is dependent on which surface is exposed, consequently modifying interface properties. Barrier height's parameters were extracted out considering the thermionic current level related to the Schottky barrier height: $I \propto exp(-q\phi_{Bn}/k_B T)$, where q is the electronic charge, k_B is the Boltzmann constant and T is the absolute temperature [35]. Considering the gate bias as grounded, Φ_{Bn} values between 0.41 and 0.75 eV were found. Although, from XRD results, one can reasonably consider two preferential growths in (110) and (101) directions, corresponding to χ^{SnO_2} values of about 5.7 eV and 5.1 eV, respectively [60], it is not possible to guarantee that those surfaces normal to the growth direction are the ones exposed in the electrodes/semiconductor's interfaces. Regarding those parameters, it is known that if $\Phi_m > \chi^{SnO_2}$, it results in a Schottky barrier and, if $\Phi_m < \chi^{SnO_2}$, an Ohmic contact is obtained. However, this dependence is not that simple due to surface/interface states intrinsic to this nanostructure, thus a Schottky barrier could be formed in both conditions [30]. In addition, when it comes to a device under gate biasing condition, a built-in potential, i.e., a variable barrier seen by carriers inside the semiconductor may be taken into account, as it is to describe our simple model.

Different conditions were then analyzed: the device (1) under positive gate bias ($V_G > 0$) and no applied source/drain bias ($V_{DS} = 0$); (2) $V_{DS} > 0$ and $V_G > 0$; (3) $V_{DS} < 0$ and $V_G < 0$ and (4) $V_{DS} < 0$, $V_G < 0$ but under UV illumination [Figure 30]. The latter requires an understanding regarding photo generated current. The third condition can be assumed as a reverse polarized diode, where the barrier height and the depletion layer width formed in between surfaces are both large enough to stop current flow, as depicted in Figure 22. However, under illumination, with corresponding wavelength energy higher than the semiconductor's band gap, e-h pairs are formed and dissociated by the electric field. As a result, free extra carriers are produced and flow in opposite directions modifying the depletion layer width and also a net density of holes at the SnO$_2$ surface is formed. Holes accumulating near the surface then are able to contribute to the conduction under this biasing condition ($V_{DS}, V_G < 0$). The ambipolarity in transistors could be described as the condition in which drain and source contacts offer no resistance for both carriers, i.e., the device can be characterized as n- and p- channel device depending on the applied voltages. In this way, when accumulated holes at the SnO$_2$ surface in our device are subjected to an external field they are ready to contribute to

the current flow composed by holes, which characterize the devices as ambipolar, since both types of carriers can contribute to the final current depending on the biasing.
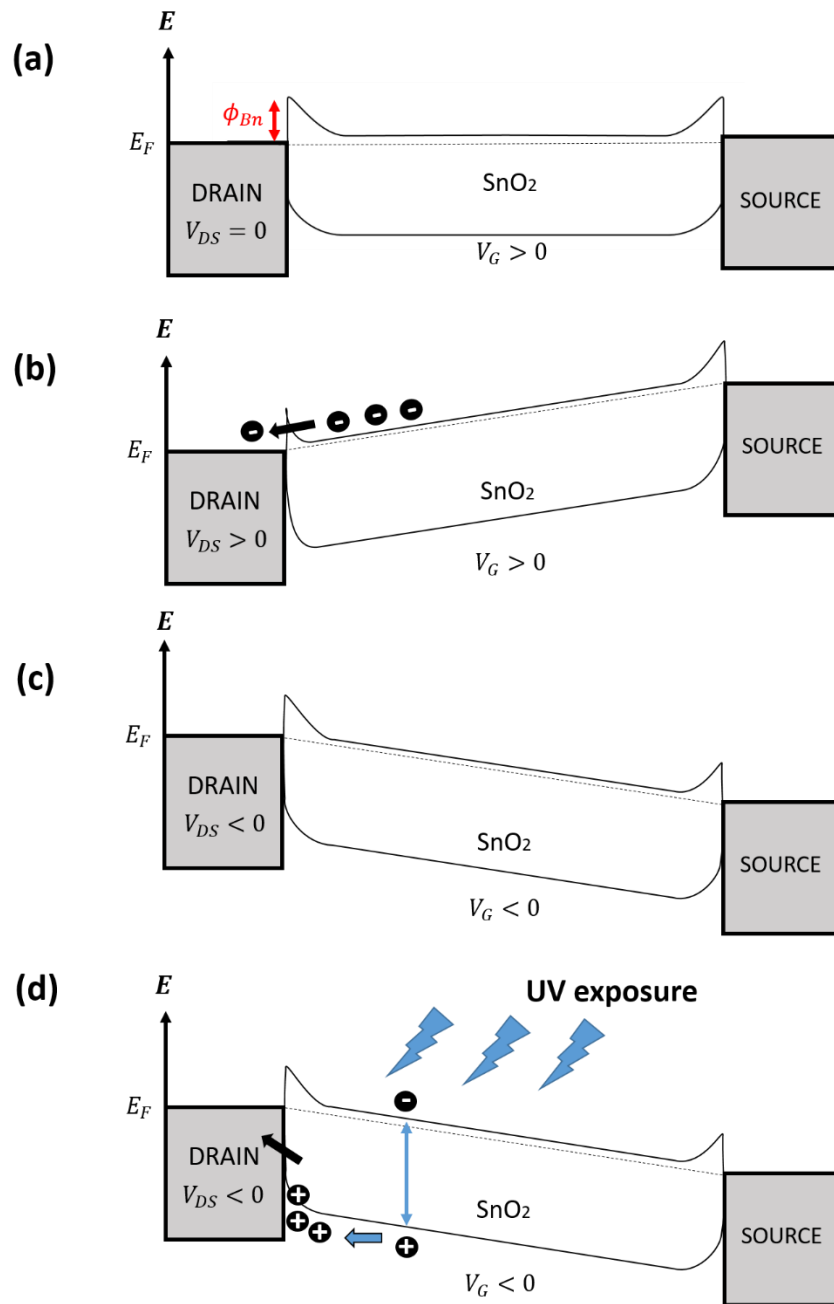
Figure 29 - A simple band model for ambipolarity effect in SnO₂NWFET is described by the band diagrams for the Metal-Semiconductor interfaces, with the related built-in potential (ϕ_B) variation (Schottky barrier), where (a), (b) and (c) are the observed operation at different gate (V_G) and source/drain (V_{DS}) bias and (d) when under ultraviolet (UV) radiation.

The metal-semiconductor junctions formed by the semiconductor and source/drain electric contacts interfaces, depicted in Figure 30 (a), (b), (c) and (d) provide some characteristics to understand the observed operation. When considering $V_{DS} = 0$ and V_S grounded (related to V_{DS} and V_G), two conditions could arise: when $V_G > 0$, electrons' accumulation is adjusted by the positive potential applied on the gate [Figure 30 (a)]. If $V_{DS} > 0$ is set, the interface capacitance thickness is lowered

and the barrier height sufficiently decreases for drain current to flow, as in Figure 30 (b). Taking a negative V_G value, $V_G < 0$, electrons are depleted from the surface and there is no contribution from the minority carriers, i.e. holes, and the previous conditions remain valid [Figure 30 (c)]. However, when the device is under ultraviolet radiation, the processes that lead to the ambipolarity effect result in $I_{DS} \neq 0$ and $I_{DS} < 0$.

In summary, besides that all seven devices investigated in this work presented transistor-like characteristics, as was expected for SnO_2, the ambipolarity effect induced by UV Light was also present. Ambipolarity is one of those effects that may direct its use for specific purposes, where a controllable separated unipolar mode can be achieved in one single device.

4.2.2. SnO$_2$ NWFET as a UV photodetector

Nowadays, one-dimensional SnO_2 based devices have demonstrated their potential application in UV sensing [4,7,14,41]. The study and development of UV photodetectors has extended beyond its usual applications in optical communication and flame detectors, gaining attention in the hospital environment and as exposure sensors. Several research topics were conducted using SnO_2 NW network [41] and single NW devices [7,14], in a metal-semiconductor-metal (MSM) or FET structures. Most of the $I_{DS} - V_{DS}$ responses reported for SnO_2 devices [4,7,14,41] were similar to the ones obtained for the samples in this work. Furthermore, due to such a difference between the device's conditions in the dark and under UV illumination, as depicted in Figure 23, it was worth to investigate their behavior as UV photodetectors. As means to do it, the same system [Figure 18] was used to acquire current as a function of time $(I - t)$ curves with and without irradiation, which enabled the acquisition of fundamental parameters to characterize the photodetector.

As described in section 2.4, it was obtained a typical response for a photodetector device [Figure 31], i.e., defined on and off states, from which it is possible to obtain rise and decay times. The rise time (τ_r) can be understood as the response time of the device to the photo excited carriers, until it reaches a plateau or a saturation region, which is the limit of photo excited carriers for the given applied bias and light source power [41]. If the time interval chosen is closer to the rise time, a saturation region may not be noticed, consequently a non-reliable fitting may be acquired. The decay time (τ_d) can be related to the rapid change in charge concentration when irradiation is ceased and may also refer to trapping and releasing charges due to Oxygen vacancies and other levels within the bandgap [61].

Figure 31 displays on/off current ratio in function of time under $V_G = 10\ V$ and $V_{DS} = 1\ V$, subjected to a 60 s pulse. The chosen gate voltage was due to its higher current value in dark condition even for an applied V_{DS} as low as 1V [Figure 20 (a)]. The time interval of 60 s was chosen because it is considerably bigger than the rise time, which was acquired by previous testing.

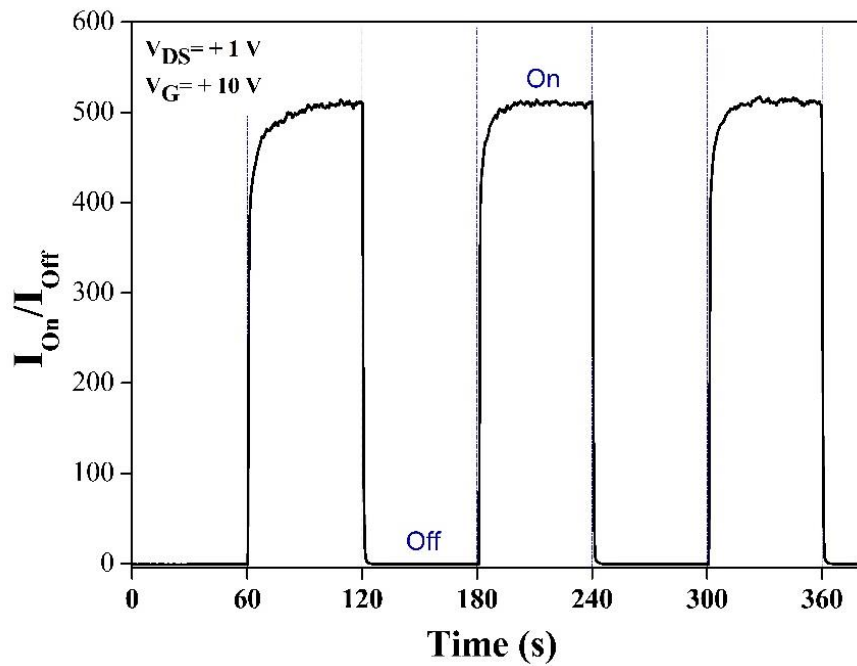*Figure 30 - I-t characteristics of the device when under UV illumination.*

The I_{on}/I_{off} ratio, when in percentage [41], was found to be of the order of 10^4 for all devices investigated. From experimental data fitting (within fitting's uncertainty $r^2 = 0.9991$), according to Eq. 2.20 and 2.21, one can acquire the parameters τ_r and τ_d. Figure 32 presents the fitting for one of the devices studied.
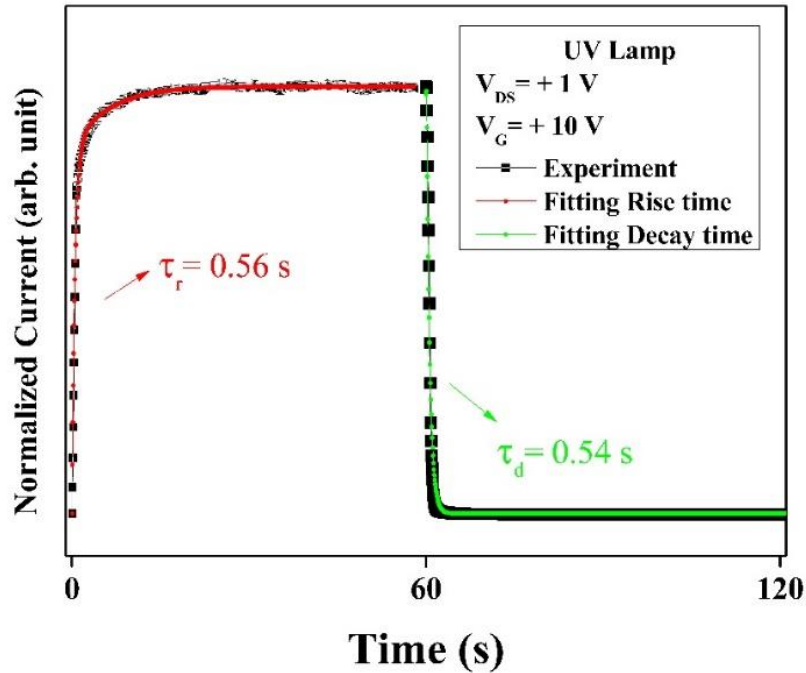
Figure 31 - Curve fitting for rise time (τ_r) and decay time (τ_d) for an operating voltage of $V_G = 10\ V$ and $V_{DS} = 1\ V$ and under UV Lamp illumination.

The rise time was found to range between 0.56 s and 0.63 (0.56 s < τ_r < 0.63 s), whereas the decay time between 0.54 s and 0.75 (0.54 s < τ_d < 0.75 s). Using a SnO$_2$ NW network as a UV sensor, in a MSM structure but synthesized through the same route chosen here, Estácio Paiva et al observed a 10^4 on/off current ratio, rise time up to 2.8 s and multiple decay times from 1 s to 100 s [41]. For a single nanowire sensor, Haiping Shi et al. reported an on/off rate of 10^2 at a 20 V operating voltage, rise time of 0.4 s and decay time of 0.6 s, using 335 nm excitation wavelength [7]. In a FET structure, a study performed by Daeil Kim et al. presented a high performance device with an array of NWs, which showed an average on/off ratio of about 10^6 [62]. Thus, by comparison to literature and some collaborative work [19,41,63], the results were found to be characteristic of a device of great selectivity and sensibility.

Even though some effects due to UV interaction are recognizable, e.g., e-h pair's formation, Oxygen's desorption from the NW's surface [Figure 24], it is quite difficult to attribute the effects noticed in the pulse curves only on their account. There are defects that can act as traps, but are not related to tin dioxide's stoichiometry, and states within the band gap that may be excited and contribute. The same is valid when the UV source is turned off. There are recombination processes that take place and, sometimes, a persistent photoconductivity effect (PPC) may be noted [63]. The latter, can be

associated to a longer or second decay time, which is basically a longer period of time necessary for the device to return to the initial dark current value or even not returning to it at all. As a consequence of this effect, the rise time may also be modified. However, in the studied single NWFET devices, the decay time was found to be of the same order of the response time, indicating a fast response in both rise and decay times.

From the results obtained, one can conclude that a single NWFET device as a UV photodetector presented similar rise and decay times' response to a single NW device [7]. Regarding the on/off ratio, it stood between the results found for the NW network [41] and NW array FET [62]. In summary, it can be considered as a fine candidate to be employed as a UV sensor.

5. Conclusions

In this work, SnO$_2$ nanowires (NW) were grown by the Vapor-Liquid-Solid (VLS) method and used to build single NW FET devices. As-grown samples went through structural and morphological analysis and seven devices single NW devices were built, with a back-gated FET architecture, by direct photolithography. All devices were electrically characterized and presented transistor-like behavior and an ambipolar effect was noted for all when under UV Light. Such effect can provide a wider range of applicability, since a controllable separated unipolar mode can be achieved in one single device. Furthermore, the devices were tested as UV sensors and presented satisfactory results. We can conclude that:

- SnO$_2$ NWs grown by VLS method presented the desired tetragonal structure and monocrystalline character, inspected by XRD and HRTEM techniques. In addition, the as-grown samples morphology of a NW with lengths of tens of micrometers and cross-section mostly displaying rectangular geometry was assured through SEM images;

- The device fabrication process by direct photolithography was proven to be efficient to build the back-gated FET architecture devices with great electrical contacts quality;

- Single SnO2NWFET's transport properties were explored, where on/off ratio, mobility and carrier density parameters were extracted, resulting in values around 10^5, lower than 0.1 cm^2/V and in the order of 10^{19}/cm^3, respectively. Schottky barrier heights were estimated, considering the gate bias as grounded, and Φ_{Bn} values between 0.41 and 0.75 eV were found. Afterwards, different conditions were analyzed: the device (1) under positive gate bias ($V_G > 0$) and no applied source/drain bias ($V_{DS} = 0$); (2) $V_{DS} > 0$ and $V_G > 0$; (3) $V_{DS} < 0$ and $V_G < 0$ and (4) $V_{DS} < 0$, $V_G < 0$ but under UV illumination. Regarding the latter, all devices presented UV induced ambipolary effect, where on/off states ratio with values of the same order were obtained and ranged from 1.1 to about 19.3. A simple band model to explain the observed behavior, i.e., describe how both types of carriers can contribute to the final current depending on the biasing was proposed.

- As a UV photodetector, the acquired I_{on}/I_{off} ratio was found to be of the order of 10^4 for all devices investigated. In addition, rise time was found to range between 0.56 s and 0.63 (0.56 s < τ_r < 0.63 s), whereas the decay time between 0.54 s and 0.75 (0.54 s < τ_d < 0.75 s). According to those results, one can assure its huge feasibility as a UV sensor.

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