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Centro de Ciências Exatas e de Tecnologia
Programa de Pós-Graduação em Engenharia Elétrica

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High Integrated Battery Monitoring System with Active Balancing up to ±10 A

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Dissertação apresentada ao Programa de Pós-Graduação em Engenharia Elétrica do Centro de Ciências Exatas e de Tecnologia da Universidade Federal de São Carlos, como parte dos requisitos para a obtenção do título de Mestre em Engenharia Elétrica.

Área de concentração: Sistemas Elétricos e Eletrônicos

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Coorientador: Prof. Dr. Ricardo Quadros Machado

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This work is dedicated to my grandfather *Wenzel Krobath* (30.8.1915 - 1.1.2004). I am pleased and proud to have met this great man.

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RESUMO

MAIER, Wenzel. **Sistema Altamente Integrado com Balanceamento Ativo e Monitoramento de Baterias de até ±10 A.** 2022. 114 f. Dissertação de Mestrado – Programa de Pós-Graduação em Engenharia Elétrica, Universidade Federal de São Carlos. São Carlos - SP, 2022.

Esta dissertação de mestrado descreve o desenvolvimento, construção e estrutura de um sistema altamente integrado, flexível e modular de monitoramento de baterias. A unidade eletrônica usa um processo de balanceamento ativo com correntes de até ±10 A para redistribuir e equilibrar a energia elétrica dentro de uma pilha de bateria. Para poder carregar e descarregar uma célula do acumulador com esta alta corrente é necessário um conversor CC/CC isolado galvanicamente, que possa transferir energia bidirecionalmente e com baixas perdas. A saída deste conversor é conectada a um multiplexador de potência que seleciona, de maneira direcionada, uma determinada célula do acumulador da bateria, permitindo realizar a medição da tensão da célula, bem como o fluxo de energia bidirecional. Isso permite que a unidade conversora CC/CC seja usada em conjunto por várias células que estão conectadas em série na bateria, reduzindo consideravelmente o custo e o espaço de instalação.

Enquanto o multiplexador tem uma construção o mais simples possível para manter baixo o custo de implementação, o conversor CC/CC bidirecional usa dois estágios de conversão simples, mas altamente eficientes, para implementar a separação de potencial e a adaptação da tensão à célula da bateria. A função e a estrutura desses dois estágios do conversor, independentes um do outro, são tratados em detalhes neste trabalho, com um modelo matemático que descreve também a interação de todo o sistema de gerenciamento de baterias. Além do mais, são apresentados e descritos todos os módulos periféricos, como a fonte auxiliar, a unidade de medição analógica, a unidade de comunicação e a unidade de controle digital do conversor CC/CC.

O desempenho do sistema proposto é comprovado por medições em um protótipo. Com base na potência de entrada e saída, a eficiência, bem como a perda de potência do conversor CC/CC, do multiplexador e de toda a eletrônica das placas foram determinadas. O sistema de gerenciamento de bateria implementado permite balancear a célula selecionada com uma eficiência de até 85 % em um curto espaço de tempo. Além disso, a medição da tensão da célula, que é particularmente importante para monitorar a bateria, foi verificada e testada. Após ajustar o sistema, é possível realizar uma medição de tensão com uma resolução de ±500 µV. Isso permite que o estado de carga de cada célula seja determinado individualmente com um alto grau de precisão.

Palavras-chave: gerenciamento de bateria, monitoramento de células, balanceamento ativo, conversor bidirecional CC/CC, multiplexador de potência

ABSTRACT

MAIER, Wenzel. **High Integrated Battery Monitoring System with Active Balancing up to ±10 A.** 2022. 114 f. Dissertação de Mestrado – Programa de Pós-Graduação em Engenharia Elétrica, Universidade Federal de São Carlos. São Carlos - SP, 2022.

This master's thesis describes the development, construction, and setup of a flexible and modular, highly integrated battery monitoring system. The electronic unit uses an active balancing process with currents up to ±10 A to redistribute and balance the electrical energy within a battery stack. In order to be able to charge and discharge an accumulator cell with this high current, a galvanic isolated DC/DC converter is necessary, which can transfer energy bidirectionally with low losses. The output of this converter is connected to a power multiplexer, which selects a desired accumulator cell of the battery stack in a targeted manner. This enables the cell voltage to be measured and the flow of energy to or from the cell. This allows the DC/DC converter unit to be used jointly by several accumulator cells connected in series, thereby reducing installation space and costs considerably.

While the multiplexer has a structure that is as simple as possible to keep the outlay for implementation low, the bidirectional DC/DC converter uses two highly efficient converter stages to implement the potential separation and the voltage adjustment to the accumulator cell. The function and structure of these two converter stages, which are independent of one another, are dealt with in detail in this work, with a mathematical model also describing the interaction of the entire battery management system. Furthermore, all peripheral modules, such as auxiliary power supply, analog measuring unit, communication and digital control unit, of the DC/DC converter module are presented and explained.

The performance of the presented concept is proven by measurements on a hardware prototype. Based on the input and output power, the efficiency as well as the power loss of the DC/DC converter, the multiplexer and the entire electronic were determined. The implemented battery management system allows the selected cell to be balanced in a short time with an efficiency of up to 85 %. In addition, the cell voltage measurement, which is particularly important for monitoring the battery, was checked and tested. After adjusting the electronic, a voltage measurement with a resolution of ±500 µV is possible. This allows the state of charge of each individual cell to be determined with great accuracy.

Keywords: battery management, cell monitoring, active balancing, bidirectional DC/DC converter, power multiplexer

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LIST OF ABBREVIATIONS AND ACRONYMS

5000+	price refers to 5000 or more units
AC	alternating current (voltage)
ADC	analog-to-digital converter
AFE	analog front-end
BOT	bottom layer of the PCB
CC-CV	constant current - constant voltage charging (discharging) method
CCM	continuous current mode
CMOS	complementary metal–oxide–semiconductor
DC	direct current (voltage)
DCM	discontinuous current mode
DNL	differential nonlinearity of ADC
EIA-485	also known as RS-485, TIA-485 or ANSI-485
ELV	extra-low voltage (IEC 60449)
ESL	equivalent series inductance of capacitor
ESR	equivalent series resistance of capacitor
EEPROM	electrically erasable programmable read-only memory
I^2C	inter-integrated circuit
ICSP	in-circuit serial programming interface (Microchip)
INL	integral nonlinearity of ADC
LC	inductor-capacitor resonant circuit
LDO	low-dropout regulator
LED	light-emitting diode
$Li_4Ti_5O_{12}$	lithium-titanate-oxide accumulator
$LiCoO_2$	lithium-cobalt-oxide accumulator
$LiFePO_4$	lithium-iron-phosphate accumulator
$LiMn_2O_4$	lithium-manganese-oxide accumulator
$LiNiCoAlO_2$	lithium-nickel-cobalt-aluminum-oxide accumulator
$LiNiMnCoO_2$	lithium-nickel-manganese-oxide accumulator
$Li_4Ti_5O_{12}$	lithium-titanate-oxide accumulator
LSB	least significant bit
LUT	lookup table
MD1	first middle layer of the PCB
MD2	second middle layer of the PCB

MIPS	millions of instructions per second
MOS	metal–oxide–semiconductor technology
MOSFET	metal–oxide–semiconductor field-effect transistor
MSB	most significant bit
NTC	negative temperature coefficient thermistor
PCB	printed circuit board
PID	proportional-integral-differential controller
PTC	positive temperature coefficient thermistor
PWM	pulse-width modulation
RC	resistor-capacitor filter circuit
RTD	resistance temperature detectors (PT1000 or similar)
SoC	state of charge of an electric battery system
SoH	state of health of an electric battery system
SoS	state of safety of an electric battery system
SMD	surface mount device
THT	through hole technology
TOP	top layer of PCB
TQFP	thin quad flat package
TVS	transient-voltage-suppression diode
UART	universal asynchronous receiver-transmitter

— Important potential labels on the primary side:

3V3	3.3 V auxiliary supply
GND	reference potential (ground)
VCC	output of low drop-out regulator LP2951-5
VZK	potential of intermediate circuit

— Important potential labels on the secondary side:

2VZK	double potential of *VZK*
3V0	switchable 3.0 V auxiliary supply
3V3	3.3 V auxiliary supply
aVCC	auxiliary supply for analog front-end stage
a3V3	analog 3.3 V auxiliary supply
aGND	analog reference potential (analog ground)
GND	reference potential (ground)

HS1	switching note at synchronous converter (full-bridge)
HS2	switching note at high-low selection circuit (full-bridge)
L1	*Line1* at synchronous converter (full-bridge)
L2	*Line2* at high-low selection circuit (full-bridge)
Out	output (respectively input) of the synchronous converter
VCC	output of VCC boost converter
VDD	output of VDD boost converter
VZK	potential of intermediate circuit

– Further label names can be read directly from the circuit diagrams.

LIST OF SYMBOLS

— General math acronyms:

$\cdot$	mathematical operator: "normal" multiplication or matrix multiplication
$\|\|$	mathematical operator: $R_1 \,\|\|\, R_2 \,\|\|\, ... \,\|\|\, R_n = \frac{1}{1/R_1 + 1/R_2 + ... + 1/R_n}$
ω	angular frequency: $\omega = 2 \cdot \pi \cdot f$
j	imaginary unit: $j = \sqrt{-1}$
s	complex frequency parameter: $s = j \cdot \omega + \sigma$, with $\sigma = 0 \rightarrow s = j \cdot \omega$
x	variable - variable over time (changes within a period)
X	variable - constant over time (constant over at least one period)
$\mathbf{X}$	matrix or vector - constant over time/frequency
$x(s)$	variable - variable over frequency
$\mathbf{x}(s)$	vector - variable over frequency
$x(t)$	variable - variable over time (equal to x)
$\mathbf{x}(t)$	vector - variable over time
$\mathbf{X}^T$	transposed matrix/vector - constant over time/frequency
$X_{'Y'}$	component designation 'Y' - e.g. R_{R1} is the resistance of resistor R1
$X_{'Z'}$	potential designation 'Z' - e.g. U_{VZK} is the voltage of the VZK potential

— Specific electrotechnical acronyms:

%	in the schematic diagrams indicates high-precision resistors
ϵ_r	relative permittivity
η	efficiency factor
μ_0	vacuum permeability: $\mu_0 = 4 \cdot \pi \cdot 10^{-7}\,\mathrm{N/A^2}$
τ_{Sync}	time constant of the synchronous converter
α	duty cycle of the synchronous converter switch Q5
β	duty cycle of the synchronous converter switch Q6
γ	duty cycle of the push-pull converter switches Q1 and Q3
δ	duty cycle of the push-pull converter switches Q2 and Q4
A_e	cross-section of EFD20 ferrite core
A_L	magnetic conductance of ferrite core
B_{max}	maximum magnetic flux density in the ferrite core
B_{sat}	maximum allowable magnetic flux density before saturation occurs
C	generally capacity (also C-rate of an accumulator cell)

E	generally energy
$f_{cut,1}$	$-3dB$ cut-off frequency of measurement amplifier stage - first stage
$f_{cut,2}$	$-3dB$ cut-off frequency of measurement amplifier stage - second stage
$f_{cut,3}$	$-3dB$ cut-off frequency of measurement amplifier stage - output
$f_{res,Sync}$	resonance frequency of the synchronous converter - LC resonant circuit
f_{sw}	switching frequency of push-pull and synchronous converter
I	generally current
I_{Δ}	ripple current in a power inductor
I_A	auxiliary variable - later be replaced by the corresponding expression
I_B	auxiliary variable - later be replaced by the corresponding expression
I_{Cell}	charge/discharge current of the accumulator cell (equal to I_{Out})
I_D	drain current of a MOSFET
I_{DC}	direct current without ripple in a power inductor
I_{leak}	leakage current between primary and secondary side of a transformer
I_{max}	maximum current that occurs during operation
I_{op}	operating current of a semiconductor
I_{Out}	output (input) current of the cell balancer circuit (equal to I_{Cell})
$I_{Set,neg}$	negative current setpoint value of the closed-loop control
$I_{Set,pos}$	positive current setpoint value of the closed-loop control
I_{Switch}	current consumption of bidirectional power switch (power multiplexer)
k	turn ratio of a transformer: $k = n_{sec}/n_{pri}$
L	generally inductance
$L_{\sigma,pri}$	transformer leakage inductance - primary side
l_{air}	air gap in the ferrite core
$L_{M,pri}$	transformer main inductance - primary side
n	generally number of turns of a coil (inductor or transformer)
n_{pri}	number of turns of a transformer - primary side
n_{sec}	number of turns of a transformer - secondary side
P	generally power
P_L	thermal power loss
Q	generally charge
Q_G	gate charge of a power MOSFET
R	generally resistance
R_{Cu}	copper resistance of a conductor path on the PCB
R_{pri}	copper resistance of a transformer - primary side
R_{sec}	copper resistance of a transformer - secondary side

R_{DSon}	drain-source switch-on resistance of a power MOSFET
t	generally time
U	generally voltage
U_{Bat+}	positive voltage of the whole battery
U_{Bat-}	negative voltage of the whole battery
U_{Cell}	voltage of the selected accumulator cell (equal to U_{U2})
U_{GS}	gate-source voltage of a MOSFET
U_{Out}	output (input) voltage of the full-bridge system
U_{Set}	voltage setpoint value for the closed-loop control
v	number of measurements

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1 INTRODUCTION

As a result of the desired and necessary decarbonization of energy generation, the use of renewable energy suppliers is increasing worldwide. Therefore, at distribute locations small power plants produce electrical energy and, depending on requirements and availability, supplies it into the power grid (smart grid). However, the generation of energy from sun, wind, and sea is subject to strong temporal and power fluctuations and typically does not correlate with the energy consumption. For this reason, the need for energy storage solutions is also increasing sharply in order to stabilize the smart grid and deliver energy at the desired time (Roberts; Sandberg, 2011; Molina, 2017; Rodriguez, 2010).

As a chemical energy storage element accumulator cells are used heavily in home batteries and large battery storage power stations (Horiba, 2014; Vartanian; Bentley, 2011; Roberts, 2010). Regardless of this, lithium-ion accumulators are also a key element for electrical vehicles (Winter; Passerini, 2011; Hannan et al., 2018). Therefore, the correct operation of the battery and especially each individual cell is crucial for the reliability and lifespan of the entire system. For this task, every battery requires a highly specialized electronic. This electronic is optimized to supervise and control each cell individually (Xing et al., 2011). For this reason, a high-precision measuring unit determines the voltages of each accumulator cell. The voltage is used to implement an overcharge and deep discharge protection and also indicates the current state of charge (SoC) for each cell. A temperature unit measures the battery temperature at various points and allows to disable or reduce the usable power if under- or over-temperature occurs (Andrea, 2010; ST, 2020; Renesas, 2018). Based on the measurements, a state of safety (SoS) and state of health (SoH) for each accumulator cell can be calculated and tracked over time (Daowd et al., 2011). By knowing every single cell voltage and by measure the charge and discharge currents of the whole battery, also a precise energy monitoring and efficiency calculation can be reached (ST, 2020; Renesas, 2018).

Nevertheless, the most important task of the electronic unit is the cell balancing process (Chang et al., 2014). An imbalance in electrical capacity between all individual cells reduce the capacity of the total battery and its operating time and, consequently, the usable power/energy. Therefore, the electronic must make a charge equalization between the cells (Barsukov, 2009; Wei; Zhu, 2009). This charge equalization can be made by several balancing techniques, with their individual advantages and disadvantages such as passive/active balancing, balancing current and time, efficiency (losses), cell measurement technology (accuracy), number of accumulator cells, etc. (Daowd et al., 2011; Qi; Dah-Chuan Lu, 2014; Omariba; Zhang; Sun, 2019). Regardless of the type of balancing, the electronic must ensure that all cells work in the optimal range at all times (Goldilocks zone - ST (2020)).

1.1 Cell Measurement

To achieve higher nominal voltages for the operation of electrical loads with higher power, single accumulator cells are connected in series. Depending on the application, 350 and more cells are connected to a common string to achieve a total voltage of up to 1600 V (Chang et al., 2014; Wei; Zhu, 2009). In this battery string, each accumulator cell must be operated within strictly defined parameters at all times to reliably avoid damage or destruction of the cell. Even leaving the safe area for a short time should be avoided, as this inevitably reduces the lifespan of the cell and, accordingly, the entire battery system (Korthauer, 2013; Buchmann, 2017).

1.1.1 Current

To avoid damage to the accumulator cells, a battery system must not be charged and discharged with excessive currents. The limits for these charging and discharging currents depend on the type of cell used (see cell data sheet information) and the number of accumulator cells connected in parallel. An exact current measurement is therefore necessary to react appropriately when the specified limits are exceeded. In addition, the current measurement (in combination with the cell voltage measurement) is the battery's level indicator. The measurement of the current as well as the time when charging and discharging the battery system provides information on how much electrical charge the cell has absorbed or emitted ($Q = I \cdot t$). Since the current value is accumulated over time, the current measurement unit must work very precisely over a wide range (from milliamperes to hundreds of amperes) and may only have a negligible offset error (Lelie et al., 2018).

Since all accumulator cells are connected in series and the current through all cells are the same, one current measurement per cell string is sufficient to monitor the entire battery. If the string only consists of a few cells (e.g. 10 cells of an electric bike), the current measurement is usually accommodated together with the cell voltage measurement and the balancing electronic on a common printed circuit board (PCB) or in a common housing/module. Batteries with hundreds of cells are frequently divided into modules, with each module having its own balancing electronic. The current measurement itself is carried out only once as a separate unit and inserted at a suitable point on the battery (preferably directly at the positive or negative battery connection). In this case, the current measurement is spatially separated from the balancing electronic and not a part of it (no common PCB).[1] Measurement data (and their timestamp) are collected via a bus system and evaluated centrally in a battery control unit.

[1] Depending on the structure of the balancer electronic, it can contain its own internal current measurement to monitor the energy balance within the battery.

1.1.2 Temperature

An essential factor for the safe operation of an accumulator cell is its temperature (Lelie et al., 2018). Apart from special lithium-ion high-temperature cells, the battery can work in an operating range of −60 °C to +60 °C (Ma et al., 2018), depending on the electrolyte used. The optimum operating temperature, where the battery can deliver its full capacity, is around 25 °C. In a cold environment, the mobility of the lithium ions in the electrolyte is restricted and the internal resistance increases sharply (Aris; Shabani, 2017). Hence, the cell can only deliver limited currents at temperatures below 0 °C. At temperatures above 60 °C (depending on the electrolyte used) the electrolyte begins to decompose chemically. It must be considered that the self-heating caused by charging and discharging currents must be added to the ambient temperature and the limit temperature is therefore reached quickly (e.g. 35 °C ambient + 25 °C self-heating = 60 °C).

For this reason, multiple temperature sensors are required to monitor the actual temperature of the battery. In order to reduce the measurement and cabling effort and thus costs, not all accumulator cells are thermally monitored. Temperature sensors are only attached to thermally relevant points on the battery. Also, for cost reasons, mainly thermistors (NTCs or PTCs) and semiconductor diodes are used, with an accuracy of ±1.0 °C being achieved. To avoid a short circuit, electrical insulation must be provided between the accumulator cells and the sensors (including measuring lines), as these parts can have different potentials. The temperature measurement circuit is usually carried out together with the balancing electronic and is therefore a part of it. The measured data are processed by the shared digital unit and can be read out via a bus system.

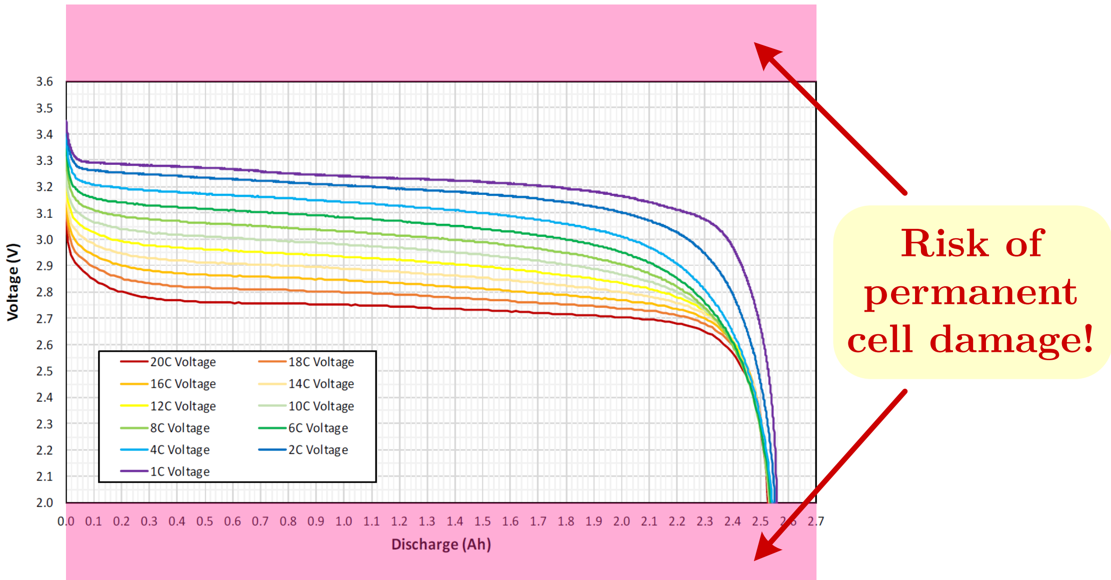
1.1.3 Voltage

The most important parameter is the cell voltage, which must remain within a maximum and minimum voltage (Andrea, 2010; Buchmann, 2017; Kien; Fowler, 2020). For example, the Figure 1 shows the discharge curve of a $LiFePO_4$ lithium-ion accumulator cell and its voltage limits. Under 2.00 V undesirable chemical side reactions begin to greatly reduce the capacity and damage the cell. Over 3.60 V internal chemical reactions also begin to destroy the cell. Thereby, the battery cell heats up considerably, which can lead to a thermal runaway and result in an uncontrollable fire in the battery (Kien; Fowler, 2020). For this reason, the safe operating area must never be left.

The values of the voltage limits depends strongly on the materials used in the cell (galvanic respectively electropotential series) and to a lesser extent on the manufacturing process.[2] A good overview of lithium-based battery technologies can be found in Hannan et al. (2018) and Buchmann (2017) while Table 1 shows the typical voltage ranges.

[2] Therefore, the voltage of the $LiFePO_4$ cell in Figure 1 deviates from the maximum achievable cell voltage (Table 1). For the correct voltage limits, please refer to the battery manufacturer's data sheet.

Figure 1 – Discharge curve of a $LiFePO_4$ cell - example



Source: adapted from LithiumWerks (2019)

Table 1 – Typical cell voltages of different lithium-based accumulator cells

cell chemistry	nominal	full charge	full discharge	minimal	comment
$LiCoO_2$	3.60 V	4.20 V	3.00 V	2.50 V	high energy
$LiMn_2O_4$	3.80 V	4.20 V	3.00 V	2.50 V	high power
$LiNiMnCoO_2$	3.60 V	4.20 V	3.00 V	2.50 V	high capacity
$LiFePO_4$	3.30 V	3.65 V	2.50 V	2.00 V	high power, safe
$LiNiCoAlO_2$	3.60 V	4.20 V	3.00 V	2.50 V	highest capacity
$Li_4Ti_5O_{12}$	2.40 V	2.85 V	1.80 V	1.50 V	long live, safe

Source: adapted from Buchmann (2017)

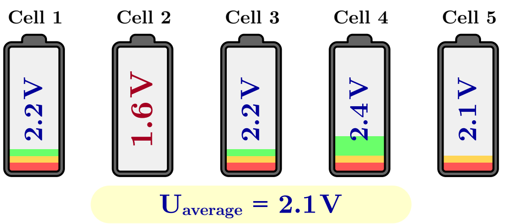
To address every accumulator technology, the balancing electronic must be able to measure the cell voltage, including reserves, in a range of approximately 1.20 V to 4.50 V. To achieve an over- and under-voltage switch-off functionality, it is sufficient to measure this voltage with an accuracy of ±20 mV. However, the voltage is important information about the cell capacity and shows the user how much energy actually the cell has. Hence, it is needfully to measure the voltage with an accuracy of ±1 mV or better (Lelie et al., 2018). This is specially true for $LiFePO_4$ accumulators types with the flat voltage curve as seen in Figure 1.[3]

This voltage measurement must be carried out separately for each cell in the string. A common voltage measurement of several accumulator cells or the entire battery stack is not possible, as this does not allow any conclusions to be drawn about the status of an individual cell. Figure 2 illustrates this difficulty, (Omariba; Zhang; Sun, 2019). While the

[3] The C-rate (C in Figure 1) indicates the charging or discharging current of an accumulator relating to its total capacity. E.g.: A 4 C discharge current of a 2.5 Ah accumulator cell will be −10 A.

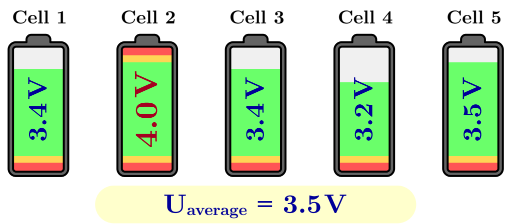
average voltage of the five cells is within the allowable range, cell 2 is out of range, which leads to its destruction (under-voltage). The same effect can be seen in Figure 3, where cell 2 is damaged by over-voltage. The balancing electronic must therefore be especially designed to record all cell voltages reliably and with great accuracy, whereby each voltage to be measured has a different reference potential as a result of the series connection.

Figure 2 – Cell under-voltage



Source: adapted from Omariba, Zhang & Sun (2019)

Figure 3 – Cell over-voltage

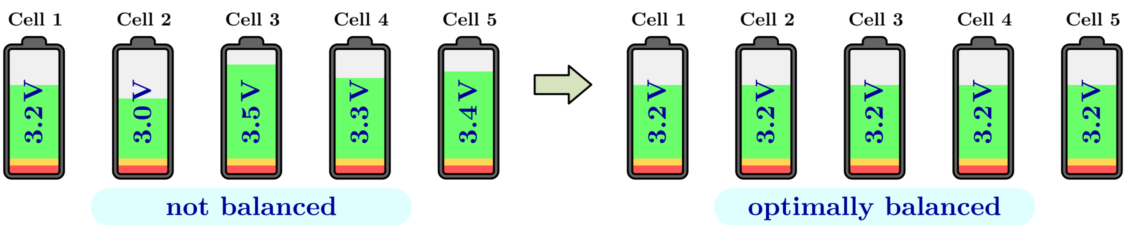


Source: adapted from Omariba, Zhang & Sun (2019)

1.1.4 Need for Balancing

An exact voltage measurement of each battery cell allows a charging or discharging process to be switched off before a cell is damaged, but does not prevent differences in cell capacities and, as a result, the voltages differing from one another. This difference in capacity is caused by production deviations, differences in cell chemistry and different operating conditions (temperature). The small effects accumulate with every charging and discharging process, which over time leads to a significant deviation in capacity and voltage between the individual cells. To compensate for these differences, active intervention by the electronic is necessary. Thereby, electrical energy is redistributed within the battery or across a cell stack (Figure 4).

Figure 4 – Balancing process - equalization of cell capacity

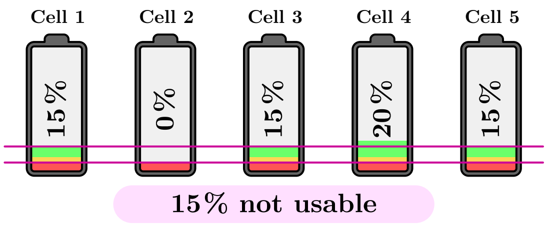


Source: by the author

The importance of cell balancing can be seen in Figure 5 and Figure 6. The charging or discharging process must be stopped when the first cell reaches the voltage limit. Without energy equalization within the battery, the other cells still have energy after the discharge process that cannot be used (Figure 5) and not all cells can be fully charged during the charging process (Figure 6). Depending on the condition and age of the battery, this loss of capacity can considerably limit the operation time of the energy storage system (Qi;

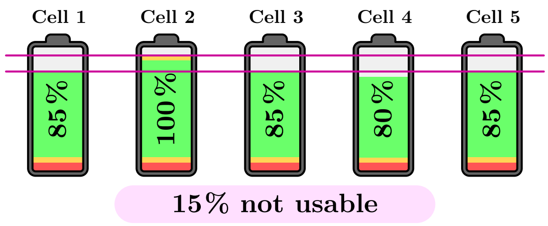
Dah-Chuan Lu, 2014; Omariba; Zhang; Sun, 2019). Balancing the battery is therefore a basic requirement for effective use of all the energy in the battery system, and is used in all devices and systems that use lithium-ion accumulators connected in series.

Figure 5 – Discharge stop



Source: by the author

Figure 6 – Charge stop



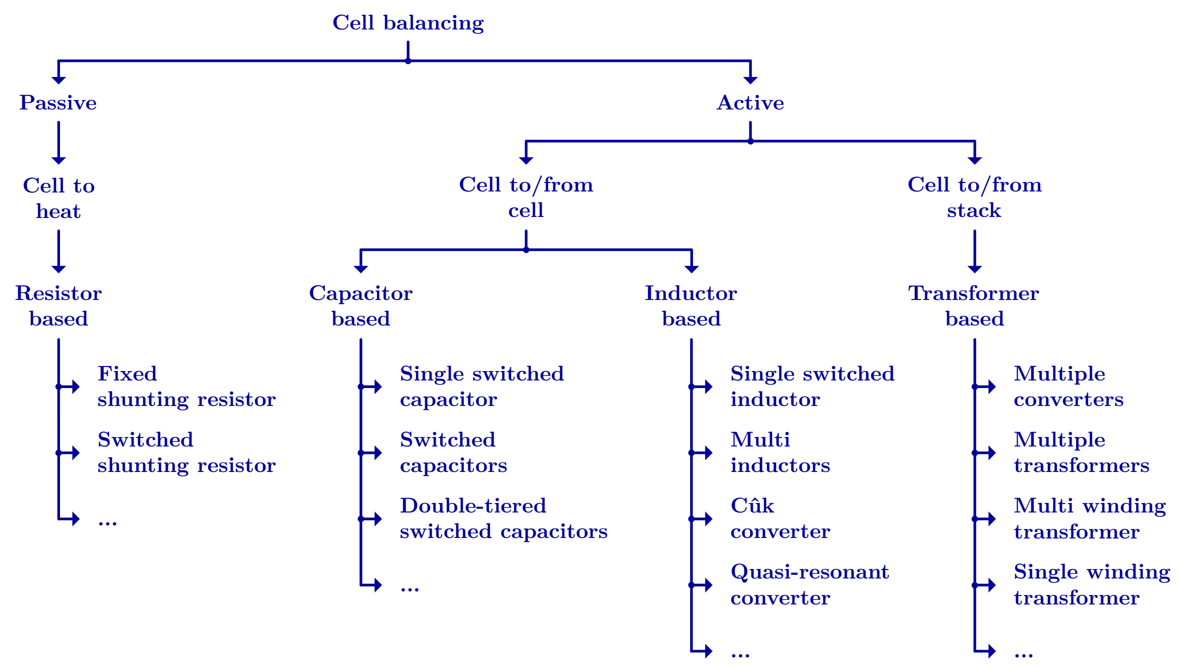
Source: by the author

1.2 Cell Balancing Techniques

Due to the intensive use of lithium-ion accumulator cells for power and energy application such as home batteries, large battery storage power stations and especially electrical cars, intensive research and development in the field of balancing techniques has been carried out in the last decades. In addition, with the further increase in high-capacity electrical energy storage systems, the need for balancing electronics with higher power and efficiency will also increase. There is always a compromise to be made among size, measurement accuracy, power, performance and costs, due to the significant differences between a battery system with ten cells for an electric bike, 100 to 200 cells for an electric car respectively a home storage system, or several 1000 cells for a power plant. For this reason, the balancing technology must be carefully selected, and the electronic must be specifically developed and designed for the battery system used.

A simple classification of different balancing methods is presented in Figure 7. The stated balancing methods were taken from Daowd et al. (2011), Omariba, Zhang & Sun (2019), whereby these represent only a small selection of possible circuit topologies (Qi; Dah-Chuan Lu, 2014; Caspar; Eiler; Hohmann, 2018). Some balancers given in the literature are modifications or combinations thereof, while others cannot be classified in the above scheme (Tashakor; Farjah; Ghanbari, 2017; Zhang et al., 2019). To better understand the advantages and disadvantages of the balancing circuits, these will be examined in more detail below using the energy transfer concept.

Figure 7 – Cell balancing techniques overview

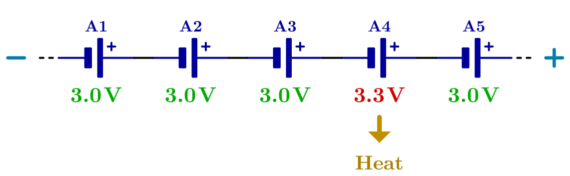


Source: adapted from Daowd et al. (2011), Omariba, Zhang & Sun (2019)

1.2.1 Cell-to-Heat

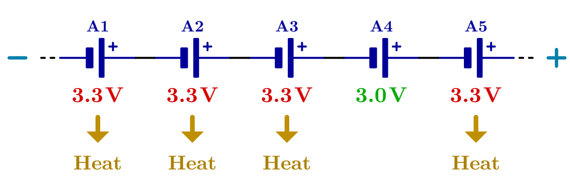
Passive or cell-to-heat balancing is the simplest and cheapest way to equilibrate a battery system. For this purpose, resistors are connected in parallel to every accumulator cell. Typically, these resistors can be switched electronically to achieve a better control and reduce power losses (Perişoară; Guran; Costache, 2018; Amin et al., 2017). If a cell in the string has more capacity and a higher voltage level than the others, the resistor can be switched on, and the excess energy is converted into heat until all cells have the same voltage (Figure 8).

Figure 8 – Single cell to heat



Source: by the author

Figure 9 – Multiple cells to heat



Source: by the author

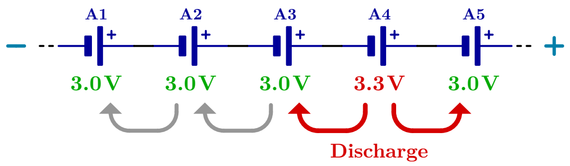
If a cell has less capacity respectively voltage like in Figure 9, the other cells must be discharge until all cells have the same reduced energy. In both cases, the energy can no longer be used, and the efficiency is therefore zero. If the resistors are not mount on a heat sink, the balancing current (discharge current) is low to keep the heating of the PCB low (typically 30 mA until 300 mA). This leads to long balancing times, especially with large battery capacities. Although this balancing technique is particularly suitable for small battery packs (electric bicycles), this technology is also used in electric vehicles.

The simple construction and, in particular, the low costs are preferred properties for using switched-resistor balancing electronics even in large energy storage systems. For this reason, most semiconductor manufacturers offer a wide range of semiconductor chips for cell-to-heat balancing (e.g. BQ76952, BQ76PL455A, MAX17852, LTC6804-1).

1.2.2 Cell-to/from-Cell

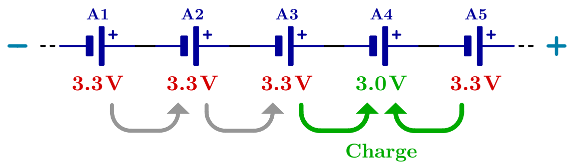
Cell-to/from-cell balancing is an active balancing technique where the balancing energy is not lost. Therefore, the excess energy of an accumulator cell is transferred to neighboring cells. These pass on part of the energy to the following cells and so on, until the same energy level respectively voltage is established in all cells. The process is bidirectional, so that accumulator cells with higher voltage are discharged (Figure 10) and cells with lower voltage are charged (Figure 11). The cell-to-cell balancing is disadvantageous if the balancing energy has to be transferred over several cells (in the worst case, from one side of the battery string to the other). In this case, additional conversion losses appear as the energy is shifted from cell to cell and partial losses occur in each stage.

Figure 10 – Cell to neighboring cells



Source: by the author

Figure 11 – Neighboring cells to cell



Source: by the author

To transfer energy from one cell to another, an energy storage element is necessary. Capacitor-based cell balancers (Ye et al., 2017; Kim et al., 2014) work like a charge pump, where energy is shuttled from one stage to another. The efficiency can be high, if the voltage of the cells are similar. Otherwise, losses in the switches reduces the efficiency drastically (Schlienz, 2007). To deliver equalizing currents in the ampere range, either high switching frequencies with corresponding switching losses or high capacitance values are necessary.[4] If smaller balancing currents are accepted (e.g. 300 mA), efficiency also decreases, since the internal consumption of the electronic accounts for a larger part of the total energy. In Barsukov (2009) an efficiency of 50 % is specified, although this value can be subject to high fluctuations depending on the design.

Inductor-based balancers (Cao et al., 2018; Moghaddam; Van Den Bossche, 2018) can achieve efficiencies of approximately 90 %. However, this efficiency is greatly reduced if the energy has to be transferred over several stages. For example, the efficiency drops to 60 % if five converter stages are involved. An advantage is that higher equalizing currents are easier to achieve than with capacitor-based balancers, but the costs rise rapidly due to the switching elements and the storage coils have to be scaled with the current. Additionally, the

[4] Electrolytic or polymer capacitors should not be used to ensure a long lifespan of the electronic.

electronic require more space. Just like with capacitive balancers, high switching frequencies and complex driver circuitry are required to control each power switch. For example, Texas Instruments Incorporated offers the highly specialized semiconductor bq78PL114, that controls the necessary power MOSFETs. If coil and capacitor are combined, a Cûk, resonant or quasi-resonant balancer can be realized that generate fewer electromagnetic radiation and switching losses (Lee; Cheng, 2005; Ye; Cheng, 2018). As more electronic components are used, the total cost of the electronic also increases.

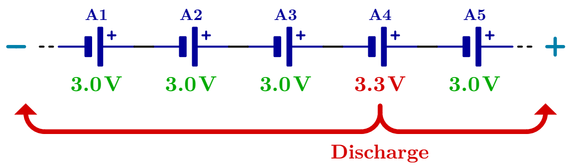
One possibility to greatly reduce the number of capacitors respectively inductors and their costs is to use a multiplexer (switch matrix), made up of individual power switches. In this case, only one single energy storage element is required (Daowd et al., 2011; Yu et al., 2020), which is alternately charged and discharged. Therefore, the power multiplexer switches the capacitor or/and inductor from one cell to another at high frequency (approximately 25 kHz to 250 kHz range). The energy is no longer transferred to neighboring cells, but can take place between any cells. Another advantage besides the reduction of the storage elements is that the cell voltage measuring unit only has to be carried out once (Lee et al., 2015). If the voltages of each accumulator cell is to be measured, the measuring circuit is connected to the multiplexer instead of the storage element (capacitor or/and coil) and the cells are measured one after the other. The disadvantage here is that a corresponding bidirectional power switch for high switching frequencies can only be implemented with great effort and at considerable cost (e.g. PhotoMOS AQZ192 or G3VM-101HR2). Furthermore, a complex regulation and control system is necessary to control the corresponding switches in correct manner.

1.2.3 Cell-to/from-Stack

To overcome the disadvantages of cell-to-cell balancers, greater technical effort is necessary. Cell-to/from-stack balancing bypasses the process of shifting energy over several stages by transferring the excess energy from an accumulator cell to multiple cells at the same time (Figure 12). The opposite way of charging an accumulator cell is also possible and shown in Figure 13. Depending on the requirements, the electronic can be designed so that either the entire battery or a part of the cell string is used. The second allows the battery to be divided into modules or stacks, which increases flexibility and modularity. Thereby, each battery stack requires its own balancing electronic and, which makes things difficult, a charge equalization between the individual battery modules.

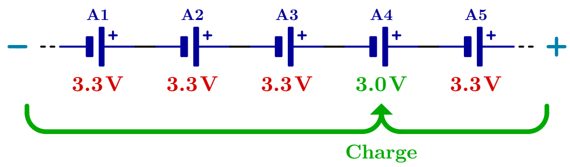
For cell-to-stack balancing, transformer-based solution in the form of a DC/DC converter are used. Flyback converters are very common because they are inexpensive and easy to set up. However, any other isolated converter topology, such as forward, push-pull, half-bridge converters etc. (Schlienz, 2007) can also be used. Depending on the design of the electronic, a unidirectional energy transfer (charging or discharging) or a bidirectional

Figure 12 – Cell to stack/module



Source: by the author

Figure 13 – Stack/module to cell



Source: by the author

energy flow (charging and discharging) can be realized. The main task is therefore to implement the requirements efficiently and at the lowest possible costs.

The most expensive but also the most flexible solution is to use one DC/DC converter for every cell (Evzelman et al., 2016; Yang; Hu; Tsai, 2020). Therefore, 100 converters would be required for 100 cells connected in series. To reduce the effort and costs at least for the control, several transformers can be controlled by a single power/control unit (Altemose; Hellermann; Mazz, 2011; Arias et al., 2015). Analog Devices Inc offers the LTC3300 semiconductor for this purpose, which uses a flyback topology to address up to six accumulator cells (Preindl, 2018).

Using a single transformer with multiple secondary windings (Bonfiglio; Roessler, 2009; Chen et al., 2020) is even more cost-effective. To select and balance a cell in the battery string, the secondary sides that are connected to the cells must be switchable (Einhorn; Roessler; Fleig, 2011; Park et al., 2014). With the appropriate design of the electronic circuit, the power switches on the primary and secondary side enable a bidirectional operation, so that the accumulator cells can be charged or discharged. In addition to the complex control of the power switches, their triggering (driver circuit) is also a challenge, as the individual switching elements are at different potentials.

The cost, size and efficiency of the transformer can be optimized if only one secondary winding is required. In addition, the control effort is also reduced. To achieve this, the output (respectively input) of the energy converter is switched to the desired accumulator cell, which should be balanced, with the aid of a power multiplexer (Lee et al., 2017; Pham et al., 2016; Nazi; Babaei, 2020). By using a DC/DC converter and a multiplexer the selection process of the cell and the high-frequency switching of the transformer system can be strongly separated from each other (Lin, 2017a; Wu et al., 2019; Kim et al., 2011). This has several advantages. First, the topology of the converter can be freely selected as the multiplexer is not integrated in it. Second, a transformer with only one secondary winding can be used, which reduces space, losses and costs. Third, it is easier to build a bidirectional DC/DC converter that can transfer energy in both directions to charge and discharge the cell. Fourth, the multiplexer and the converter can be developed separately from one another and optimized for efficiency and/or costs. Fifth, a power multiplexer can be implemented more easily if the switching process can be done at low frequency (10 Hz to 1 kHz range). And finally, it is sufficient to implement the cell voltage measuring unit only once and to scan the individual cell voltages successively with the multiplexer. The main disadvantage for the implementation of a power multiplexer is again the high costs for the bidirectional power switches, since these must be able to block voltages and conduct currents in both directions like a mechanical relay.

The AS8506C battery cell monitor and balancer from ams AG includes a bidirectional switch matrix for addressing up to seven accumulator cells. However, this semiconductor only allows a balancing current up to 100 mA, since all switching elements are combined in one small chip. Texas Instruments Incorporated offers a solution where higher currents are possible. The semiconductors EMB1428Q (switch matrix gate driver) and EMB1499Q (bidirectional DC/DC controller) allows also to balance seven cells. In addition to the control chips, corresponding power MOSFETs are required, which form the actual power multiplexer (e.g. reference design TIDA-00239 and TIDA-00817). Due to the cost of the MOSFETs and especially the control semiconductors (and the dependency on one manufacturer), this solution offers only minor advantages over a multi-winding transformer solution, as described in Einhorn, Roessler & Fleig (2011).

1.2.4 Cell-to/from-Auxiliary-Source

Cell-to/from-auxiliary-source balancing (not shown on Figure 7) is very similar to the cell-to-stack balancing. But instead of using the entire battery respectively a battery module as a source (or sink) for energy transfer, an auxiliary supply is used (Figure 14 and Figure 15). This supply has usually a low voltage of, for example, 12 V and must be able to deliver and absorb electrical energy (depending on the balancing circuit). Therefore, a battery such as that founds in vehicles is typically used for this source. In electric cars, this “starter battery” supplies numerous of low-power consumers such as board computer, entertainment, lighting, ventilation, etc. In the case of a home battery or a large battery storage power station, this supplies cooling devices, ambient sensors and display systems, etc. An example for a balancer circuit with a +12 V auxiliary supply input are the reference designs TIDA-00239 and TIDA-00817 from Texas Instruments Incorporated.

Figure 14 – Cell to auxiliary source

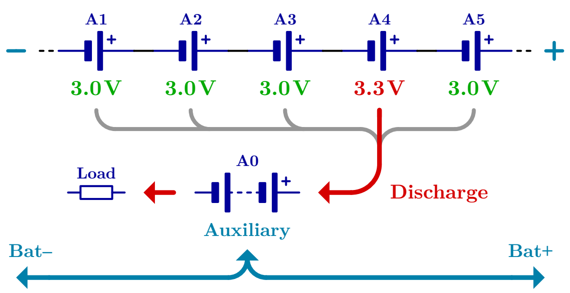


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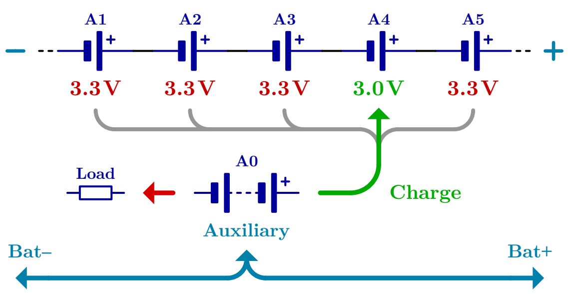
Figure 15 – Auxiliary source to cell



Source: by the author

The auxiliary power supply is typically connected to the high-voltage battery via an own high-voltage, bidirectional DC/DC converter and allows energy to be exchanged between the two battery systems. Therefore, the energy transfer between a cell and the entire battery always takes place via two steps (high-voltage DC/DC converter and balancer electronic). Although this reduces the efficiency slightly (approximately −2.5 %), it enables greater flexibility and modularity of the individual electronic units. One advantage is that the high-voltage, bidirectional DC/DC converter can be optimally designed for the voltage range and the power requirements of the high and low voltage batteries, whereby efficiencies of up to 97 % can be achieved. For the balancing electronic, a universal voltage input of around 12.00 V (approximately 8.00 V to 16.00 V) is sufficient and does not have to be adapted to the battery system every time. Another advantage is that balancing energy can be exchanged directly between battery modules or stacks thanks to the +12 V supply bus (Evzelman et al., 2016; Preindl, 2018). Hence, an extra balancing unit between the modules is not necessary.

1.2.5 Technology Comparison

The different balancing techniques are difficult to compare, as the functionality depends heavily on the design of the electronic circuit used. A simple orientation with advantages and disadvantages is given in Table 2. It should be mentioned that the numerical values in the table are only a rough estimate and can vary widely.[5]

Table 2 – Comparison of cell balancing techniques

	resistor based	capacitor based	inductor based	transformer based
discharge cell	yes	yes	yes	yes
charge cell	no	yes	yes	yes
balancing current	< 0.3 A	$0.3 - 1.5$ A	$1.0 - 10$ A	$1.0 - 10$ A
maximum power	≈ 1.5 W	≈ 6.0 W	≈ 40 W	≈ 40 W
efficiency	0 %	$25 - 75$ %	$60 - 90$ %	≈ 85 %
flexibility	poor	neutral	neutral	good
control effort	simple	simple	neutral	complex
circuit complexity	simple	neutral	neutral	complex
relative costs	low	neutral	high	high

Source: by the author

[5] The large variation in efficiency of capacitor and inductor-based solutions depends on the number of converter stages through which the balancing energy must ultimately be transferred.

1.3 Literature review

As stated in section 1.2, a part of the electrical energy is always lost during the balancing process. This particularly applies to resistor-based balancing solutions, in which all excess electrical energy is converted into heat. Although the energy converter stage of a capacitor- or inductor-based balancing system has a high degree of efficiency, a large part of the energy is also lost in these solutions if the balancing energy has to be shifted over several converter stages. The best energy conversion efficiency is obtained with transformer-based balancing circuits. These circuits use isolated DC/DC converter topologies and act directly on the accumulator cell to be balanced.

For reason of cost, it is not possible to provide a separate energy converter circuit for each accumulator cell. Solutions with numerous transformers or a multi-winding-transformer are also ruled out, as these specially adapted passive components are expensive. Therefore, it seems promising to use a single winding transformer solution that uses a multiplexer circuit to directly select the cell to be balanced. The power multiplexer consists of individual switches and uses a structure as specified in the work by Lin (2017a), Lin (2017b), Kim et al. (2012) and Pham, Duong & Choi (2020). As shown in Shah, Murali & Gandhi (2018), Erdoğan et al. (2019), Lasić et al. (2020) and Qi et al. (2021) the number of power switches can be reduced to a minimum in order to save costs. Thought, depending on the switch status, the polarity of the voltage must be adapted to the multiplexer (polarity reverser).

For the multiplexer-based solutions, any DC/DC converter circuit can be used as an energy converter, whereby two basic conditions must be met. Firstly, a galvanic isolation is absolutely necessary to separate the cell potential from the auxiliary supply potential and secondly, the voltage must be adapted to the accumulator cell.[6] Many scientific publications (e.g.: Imtiaz, Khan & Kamath (2011), Kim et al. (2012), Perișoară et al. (2019) etc.) use a simple flyback converter topology to implement potential isolation and voltage adjustment in one unit. The disadvantage here is the voltage drop at the rectifier diode and the unidirectional operation of the converter. So that the accumulator cell can be charged as well as discharged, two flyback converters are provided in the work Kim et al. (2011), Hoque, Hannan & Mohamed (2015), Lee, Choi & Kang (2019), Hannan et al. (2017) and Qi et al. (2021). The double effort can be avoided if a bidirectional converter is used as shown in Erdoğan et al. (2019), Lee et al. (2017), Qi et al. (2021) and Song et al. (2018). In addition, efficiency increases as the output diode is replaced by a switching element. A major disadvantage is that a bidirectional flyback converter requires more complex measurement (feedback signal) and control.

Energy transfer in both directions can also be implemented with other converter topologies. Depending on the power and area of application, forward, push-pull, half/full-bridge and resonance converters are used to transfer the desired energy to or from the

[6] In addition, the balancing current for charging and discharging the cell must also be limited.

battery stack. Corresponding scientific work in this area has been carried out over the past few years by Lin (2017a), Daowd et al. (2014), Shi & Song (2019), Wu et al. (2019), Nazi & Babaei (2020), Lasić et al. (2020), Qi et al. (2022), Liu, Lu & Wang (2019), Gong et al. (2018) and Uno & Yoshino (2021). What all this work has in common is that the galvanic separation and the voltage adjustment are carried out in one step, which requires a complex measurement, regulation and control.

2 OBJECTIVE

Balancing the battery with low power is already reaching its limits, as the efficiency is low and the time for balancing becomes too long. Balancing with higher power also enables a weak cell in the battery system to be actively supported. For this purpose, part of the required power is not made available by the cell but by the balancing electronic, which reduces the load on the cell. For example, the service life of the accumulator cell can be increased by lowering the internal temperature by reducing the load. This is reflected in a longer lifespan of the entire battery system which reduces the need for repair and maintenance (battery replacement) and the resulting waste (old, used batteries), which leads to significant cost savings.

Thus, the objective of this project is to develop a functional, power and cost optimized prototype of a battery management system, whereby the energy transfer takes place in two independent power converter stages. This makes it possible to use a simple electronic circuit for the bidirectional energy transfer via the galvanic insulation gap. In addition, the second stage, which is necessary for voltage adjustment, can immediately provide the correct voltage polarity for the power multiplexer (polarity reverser). Both converter stages can thus be optimized independently of one another in terms of costs and efficiency. In addition, due to the uncomplicated converter structure, only simple control signals are required. This makes it easier to implement a closed-loop control to regulate the flow of energy in both directions.[1]

Since more and more high-capacity accumulator cells respectively battery systems are used, the two-stage DC/DC converter module should provide a current of up to $\pm 10\,\mathrm{A}$ for both charging and discharging a selected accumulator cell. The entire electronic circuit structures used have a large influence on the performance, the losses respectively the efficiency and the costs of the balancer. For this reason, this work should not only describe the energy transfer for the balancing process in a mathematical way, but also include all hardware parts of the energy converter such as measurement, monitoring, communication and auxiliary power supply to represent an overall system. The prototype set-up of the active battery management system and especially the DC/DC converter unit with all its peripheral modules allows a quantitative statement to be made about the efficiency. For this purpose, the power loss and efficiency of the implemented two stage energy converter, the power multiplexer and ultimately the entire electronic system should be measured. Since the cell voltage measurement is of particular interest, it should also be checked.

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[1] Although a real-time algorithm/software is required to control the electronic, the software is not described in this work, as this would go beyond the scope of the work.

With a voltage of around 2.00 V to 4.50 V volts and a balancing power up to 45 W, this electronic system enables all common lithium-based battery technology to be operated. To make the battery management system interesting for electric vehicles, attention should also be paid to the small size of the electronic when implementing the hardware. The developed battery management system should be the basis for a new generation of industrial and automotive active battery management system solutions to monitor and balance high-power battery storage systems.

3 TEXT EXPLANATIONS

For an easier reading of the document and a better understand of the described electronic and their implementation, additional text details and explanations are given here. These text distinctions apply throughout the document.

- The entire electronic require the +12 V auxiliary source not only to charge and discharge the desired accumulator cell, but also to supply all circuit parts with electrical energy during start-up and operation. For this reason, the +12 V auxiliary source can be viewed as the main power supply and is therefore also referred to below as the +12 V main supply.

- The component designations from the chapter 6, which number the components on the circuit board, are not related to the components in chapter 4, chapter 5 and chapter 7. The component names from the DC/DC converter board (chapter 6) were created automatically by the layout program to link the circuit diagram and the printed circuit board with each other and are therefore only used there. As example, the resistor R1 in chapter 6 divers from the resistor R1 in all other chapters and is not the same component.

- Although the flow of energy is bidirectional, the auxiliary power supply side is referred to as the primary side and the battery stack side is referred to as the secondary side throughout this document. The designation “input” or “output” refers to the flow of energy from the auxiliary power supply (+12V main supply) to the accumulator cell, which is balanced regardless of whether the flow of energy is really in this direction or not.

- Since the DC/DC converter board has a potential separation, different label names are used for the voltage potentials on the primary and secondary side. All label names on the primary side are flanked by two asterisks (* symbol), while the label names on the secondary side are missing these. For example, the label **GND** denotes the ground reference on the primary side. *GND* without asterisks is the ground reference for the secondary side.

4 TECHNICAL CONCEPT

In order to balance high-capacity battery systems in a short time, large balancing currents are necessary. For example, if an accumulator cell with 100 Ah and a deviation of ±5 % is to be balanced within half an hour, a charging respectively discharging current of ±10 A is needfully ($10\,\mathrm{A} \cdot 0.5\,\mathrm{h} = 5\,\mathrm{Ah}$). This time also increases accordingly as the variance increases due to cell aging. With a possible cell voltage between 2.00 V and 4.50 V (including voltage drop on the balancing wires), the balancer electronic must be designed for a maximum output of 45 W. This output power, which is high for a balancer, can only be provided efficiently utilizing a transformer-based balancing solution (section 1.2). For cost reasons, the energy converter is switched directly to the cell to be balanced with the help of a power multiplexer. The time-sharing operation extends the balancing time when several accumulator cells are to be balanced, but allows the entire power to be allocated to one cell, if necessary. In this way, an accumulator cell that is weak can be supported during regular operation of the battery system. To enable maximum flexibility and modularity, cell-to/from-auxiliary-source balancing technique should be used (subsection 1.2.4).

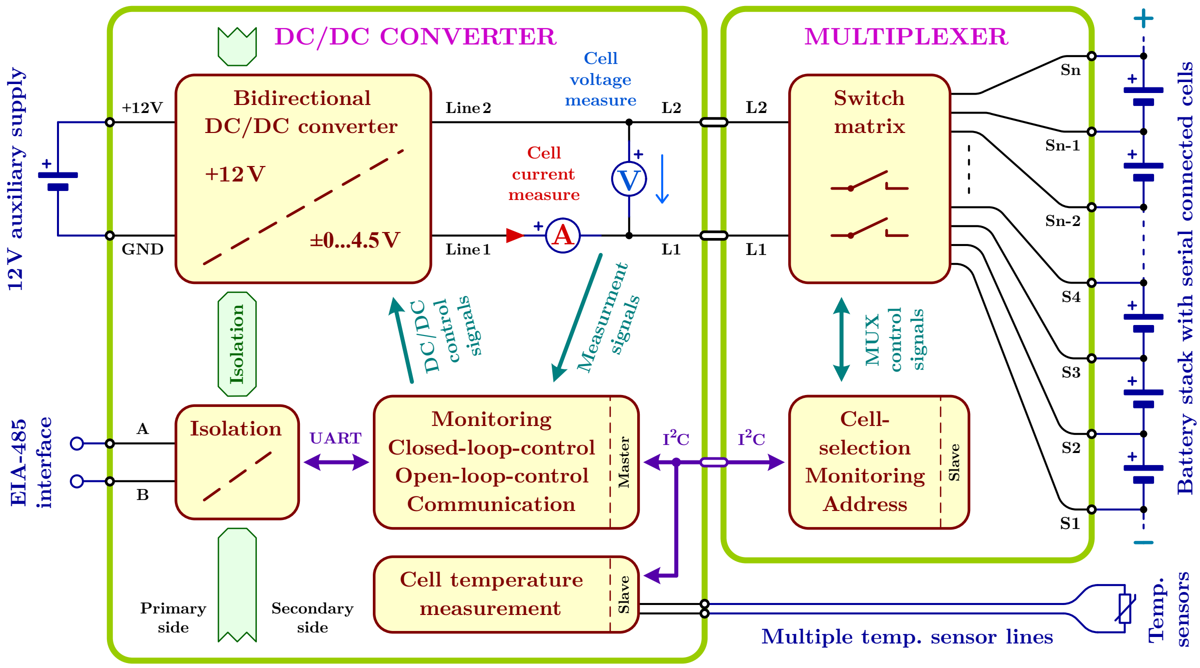
4.1 Overview

To obtain a compact and modular design of the electronic, a bidirectional DC/DC converter and a power multiplexer are used as the internal structure. If the electronics are designed correctly and is highly optimized, this allows easy selection of the cell to be balanced, good control of the power flow and a high level of efficiency. A basic block diagram of the electronic system is presented in Figure 16 with the +12 V auxiliary supply and the DC/DC converter on the left side and the multiplexer with the battery stack to be balanced on the right side. Because of the strong separation in an energy transfer unit (DC/DC converter) and a cell selection unit (multiplexer) both electronic parts can be built on two independent printed circuit boards (green areas).

The DC/DC converter board needs some specific functions to meet all requirements and to work well-matched together with the power multiplexer. Due to these requirements, a finished industrial DC/DC converter module cannot be used. All internal energy converter stages had to be specially developed for the application. The most important functions are:

- precise voltage measurement unit to meter the cell voltage
- current measurement unit to monitor the balancing process
- multichannel cell temperature measurement unit
- digital control unit for signal processing and monitoring

Figure 16 – Basic block diagram of the balancer electronic



Source: by the author

- potential separation between primary and secondary side
- bidirectional energy transfer up to ±45 W
- low-power dissipation respectively high efficiency (approximately 90 %)
- wide input voltage range from +7.50 V to +16.50 V (nominal +12.00 V)
- polarity selectable output voltage – is required by the multiplexer
- selectable, regulated output voltage up to ±4.50 V (maximum ±4.80 V)
- selectable current limitation up to ±10.00 A (maximum ±12.50 A)
- digital closed-loop control for the internal power stages
- serial I²C-master communication interfaces for slave modules (e.g. multiplexer)
- EIA-485 serial two-wire communication interface for higher-level control
- small form factor
- cost optimized

To achieve a good efficiency for the whole system, the multiplexer circuit with the bidirectional power switches must also be strongly optimized. This is only possible by built up the electronic especially for the balancing application. To achieve this, the multiplexer board must fulfill the following:

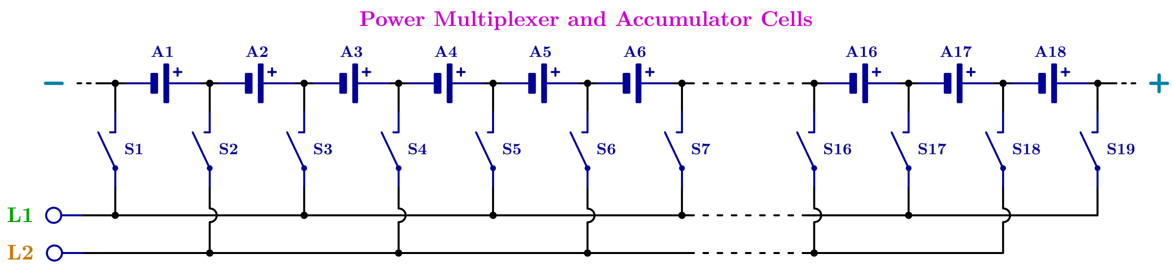
- no mechanical contacts to increase lifespan
- very little influence on the cell voltage measurement
- bidirectional current conduction up to ±10.00 A (maximum ±12.50 A)
- bidirectional blocking voltage up to ±80 V (18 cells)
- possible blocking voltage up to ±120 V (24 cells)

- low-power dissipation respectively high efficiency (> 90 %)
- digital control unit for cell selection
- bidirectional power switch supervision
- detection of overload / thermal cut-out
- voltage, temperature and status monitoring
- setting option for address or basic functions (solder jumper)
- serial I^{2}C-slave communication interface for the DC/DC converter board
- small form factor
- cost optimized

4.2 Power Multiplexer

A key technology to select the desired accumulator cell and to transferring energy to or from the cell is the power multiplexer. Figure 17 presents the structure of the multiplexer, in which *n+1* power switches will address *n* cells. For example, cell A3 can be selected by closing S3 and S4. In this case, the negative pole of A3 is connected to *L1* (also referred to as *Line1*) and the positive pole of the cell connected to *L2* (also referred to as *Line2*). *L1* can also be positive, depending on which switches are closed respectively which cell is selected.[1] Using only one power switch to select the positive pole (e.g. S4 for A3) and the negative pole (e.g. S4 for A4) of a cell makes it possible to reduce the number of power switches required and consequently also the costs. The disadvantage is that the polarity between *L1* and *L2* can be positive as well as negative. The DC/DC converter must therefore also be able to generate/provide a positive or a negative voltage at the output.

Figure 17 – Power multiplexer structure



Source: by the author

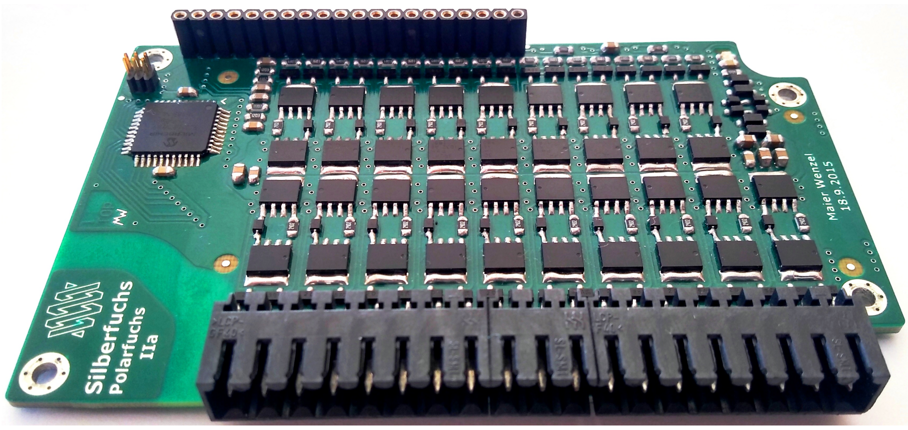
The most important point for controlling the switching elements is that two switches on the same line (*L1* or *L2*) must never be closed at the same time. This would cause a catastrophic short circuit and not only destroy the electronic completely, but also trigger a cable fire. The multiplexer structure theoretically allows also several cells to be selected at the same time, but this results in a higher voltage which the DC/DC converter actually

[1] E.g.: S4 and S5 closed → accumulator cell A4 is selected → *L1* is positive, *L2* negative.

cannot handle.[2] For this reason, only the switches S(n) and S(n+1) may be activated simultaneously for the developed electronic.

The power switches which are used for the multiplexer must be able to block both positive and negative voltage and also be able to conduct currents in both directions with minimal losses. In addition, it must be possible to select the blocking or conducting condition targeted utilizing a control signal. Theoretically, different technologies can be used to implement a bidirectional switch. The most well-known switching element, which can block or conduct voltages and currents in both directions in a controlled manner, is the mechanical relay in all of its designs (e.g. load relays, signal relays, reed relays, etc.). In addition, there is a large range of semiconductor relays (solid-state respectively photo-MOS relays), which emulate the switching function of mechanical relays.[3] When using a solid-state relay for the multiplexer shown in Figure 17, it is essential that the switch has a very low switch-on resistance and that it has no influence on the measurement of the accumulator cell voltage.[4]

Figure 18 – Power multiplexer board Polarfuchs IIa



Source: by the author

For this reason, a power multiplexer board was specially developed for the active battery management system, which contains 19 bidirectional semiconductor switches (Figure 18). Each switching element has a switch-on resistance of approximately 22.5 mΩ, whereby the copper resistances of the PCB and the input/output connector have already been considered. In addition to the bidirectional switches, numerous temperature sensors (19 pieces) and a microcontroller are implemented on the circuit board. The microcontroller not only selects the desired switches (respectively accumulator cell) but also monitors several analog signals (voltages and temperatures) and takes over communication with the DC/DC converter board. For this, the entire circuit consumes a maximum of 25 mW from

[2] For example, cells A3, A4 and A5 are selected with a total voltage of around 10 V ($3 \cdot 3.3$ V) when switches S3 and S6 are closed.

[3] The solid-state relay must not have a thyristor structure, as this cannot switch off any direct current and a simple MOSFET also cannot be used because it cannot block the current in both directions.

[4] The power multiplexer used uses “Wenzistor” semiconductor switches specially developed for this task.

the 3.0 V supply (control system) and 84 mW from the *VDD* auxiliary supply (please refer subsection 6.5.5). It should be mentioned that the multiplexer board is designed as an attachment board and is plugged directly onto the DC/DC converter board.

The actual hardware with the developed printed circuit board allows addressing 18 accumulator cells with a total string voltage of up to 80 V. The basic multiplexer circuit in Figure 17 can be extended by additional switches to address more accumulator cells. However, the breakdown voltage of the bidirectional switches must be adapted to the maximum occurring string voltage (total voltage of the battery module). This increases the costs or the switch-on resistance of the individual switches. A higher resistance reduces the efficiency so that it is not wise to control more than 24 cells directly via the multiplexer. For this reason, the switching elements must have a blocking voltage of 100 V ($LiFePO_4$) or 120 V (cells with 4.20 V full charge voltage - Table 1). Since voltages up to 120 V are viewed as extra-low voltage (ELV in IEC 60449), no special precaution are required for maintenance personnel when working on a single battery module up to 24 cells connected in series.

Due to the simple functionality of the power multiplexer, the exact structure of the electronic circuit and its implementation on the PCB is not shown in this work. It is sufficient to consider the multiplexer as a switch matrix, as presented in Figure 17, consisting of electromechanical relays with an switch-on resistance of 22.5 mΩ.

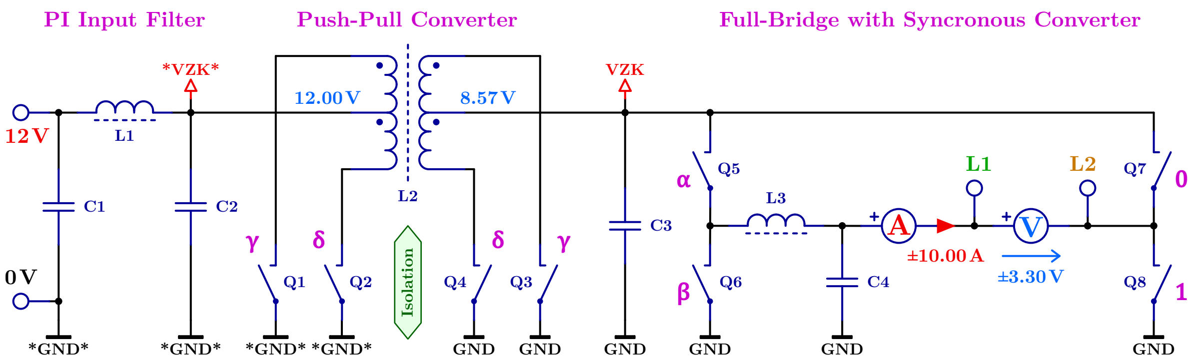
4.3 DC/DC Converter

The DC/DC converter system is specially designed to transfer electrical energy from the +12 V auxiliary supply (main supply) to the accumulator cell and vice versa. For this purpose, two bidirectional energy converter stages and a noise-cancelling input filter are necessary (Figure 19). The division of the energy conversion into two sub-areas enables easier controllability and greater flexibility compared to a single-stage converter such as a flyback topology. Both the electrical isolation and the voltage/current adjustment work independently of each other. This makes it possible to optimize the transformer L2 and the storage choke L3, shown in Figure 19, separately and to use different switching frequencies for these two power stages.

4.3.1 PI Input Filter

The push-pull converter stage as well as the synchronous converter of the full-bridge circuit generate strong switching noise (voltage and current ripple). While this noise is already eliminated at the output by L3 and C4 (Figure 19), a filter is required at the input of the DC/DC converter unit. This input filter is intended to prevent electromagnetic interference emissions from being radiated through the connection cable. For this purpose, L1, C1 and C2 form a PI filter (left side in Figure 19), which ideally allows direct current

Figure 19 – DC/DC converter structure



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to pass but attenuates high-frequency signals. To achieve sufficient damping, the cut-off frequency of the filter must be at least half a decade below the typical switching frequency of the power converter stages (at least 120 kHz). While C2 of the PI filter serves as a DC-link capacitor and is intended to stabilize the **VZK** potential, C1 and L1, with their low-pass behavior, reduce the voltage and current ripple at the input connection. In doing so, C1 and L1 form a resonance circuit and without any damping this circuit will generate an extensive voltage rise that can damage the electronic. For this reason, additional resistors are necessary to guarantee sufficient damping of the circuit. Figure 20 shows the L1/C1 filter stage and two damping resistors R1 and R2. While R2 is a SMD resistor mounted on the printed circuit board, R1 represents the resistance of the main connection cable. Therefor, R_{R1} depends on the length and cross-section of the cable.

Figure 20 – L1/C1 plus damping resistors

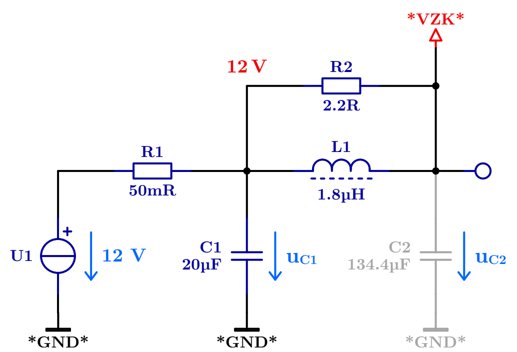

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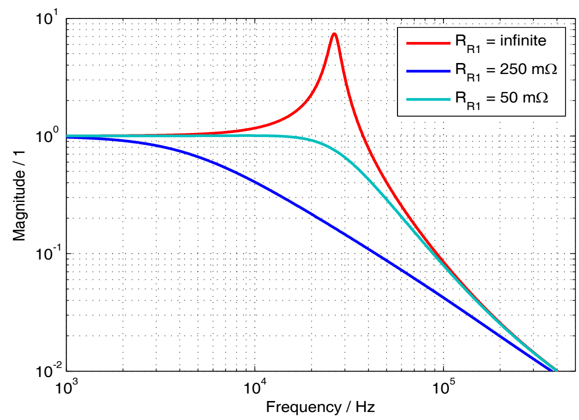
Figure 21 – L1/C1 - amplitude response



Source: by the author

Figure 21 presents the amplitude response of the circuit diagram from Figure 20. The red curve shows that R_{R2} with 2.2 Ω and without R1 is not enough to dampen the system sufficiently. There is a voltage rise of approximately 17.5 dB at the resonance frequency of 26.5 kHz and a single excitation in this area would lead to a decaying oscillation. However, if the resistance of the connection cable considered, the behavior changes completely.

As long as R_{R1} is less than $250\,\mathrm{m}\Omega$ (cyan-colored curve), the attenuation is sufficient to prevent excessive voltage over the whole frequency range. With a typically two meter long $1.5\,\mathrm{mm}^2$ cable (around $50\,\mathrm{m}\Omega$) and the specified $2.2\,\Omega$ for R_{R2}, good damping can be achieved over a wide frequency range (blue curve in Figure 21). The curves from Figure 21 are calculated by equation (1). As can be seen in this equation, the attenuation of the filter also depends on the ratio of R_{R1} and R_{R2}. Thus, by adapting R_{R2}, the circuit can be optimized for the main connection cable used.

$$\frac{u_{C1}}{u_{C2}} = \left| \frac{j \cdot \omega \cdot L_{L1} + R_{R2}}{-\omega^2 \cdot L_{L1} \cdot C_{C1} \cdot R_{R2} + j \cdot \omega \cdot L_{L1} \left(1 + R_{R2}/R_{R1}\right) + R_{R2}} \right| \tag{1}$$

For the switching frequency of 120 kHz used in the converter stages, the filter achieves a damping of at least 95 % (Figure 21). This is sufficient so that all noise on the main connection cable is less than 50 mV. At higher frequencies, however, the filter effect is lost due to parasitic capacitances on the printed circuit board (capacitive coupling). To suppress also frequencies greater than 5.0 MHz a ferrite choke on the cable can be helpfully.

4.3.2 Push-Pull Converter

Since the potentials of the +12 V auxiliary source and the cell to be balanced are different, an electrical potential separation must be implemented. For this reason, the push-pull converter stage in the middle of Figure 19 separates the entire electronic unit into a primary and a secondary side. Compared to other isolated converter topologies, the push-pull converter circuit has several advantages such as simplicity, high efficiency, low emissions, good immunity, easier transformer choice and a smaller transformer (Kamath, 2020).

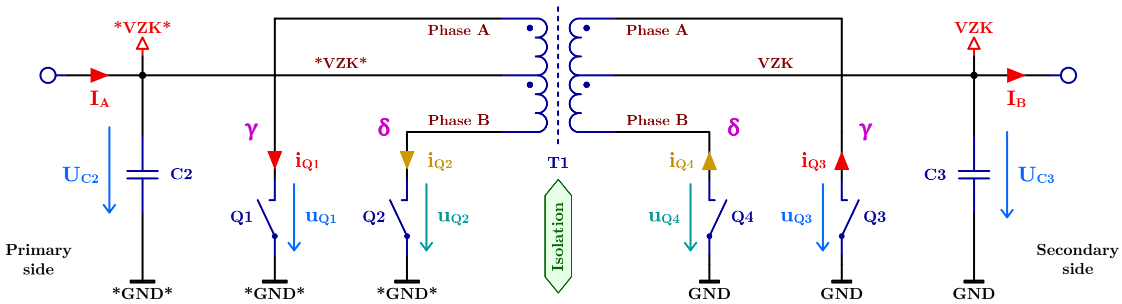
The typical push-pull converter topology uses a transformer with center taps and two power switches on the primary side to generate an alternating magnetic flux in the transformer. The magnetic flux transfers the energy to the secondary side, where two power diodes rectify voltage and current so that a DC voltage is available for the load. In addition, a storage joke is integrated at the output to smooth the current. Output voltage and power can be regulated via the duty cycle of the power switches on the primary side.

The push-pull converter used for the described battery management system is a modification of the typical push-pull converter circuit. These modifications allow for better efficiency, bidirectional energy transfer and much simpler control. In addition, the power inductance, which smooths the current, can be saved.[5] Figure 22 shows the basic circuit diagram with idealized components. For a simple consideration, the cooper resistance, the leakage and the main inductance of the transformer as well as the switch-on resistance of the switching elements can be neglected.

As can be seen in Figure 22, the primary and secondary circuits are built up in the same way respectively in mirror-inverted. The switches Q1/Q3 and Q2/Q4 are controlled in

[5] This inductance “moves” quasi to the full-bridge circuit.

Figure 22 – Push-pull converter structure - idealized



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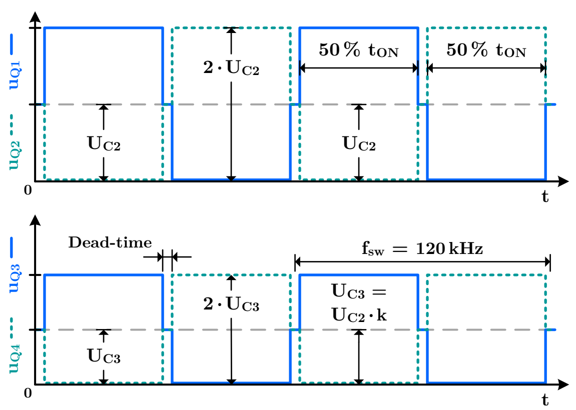
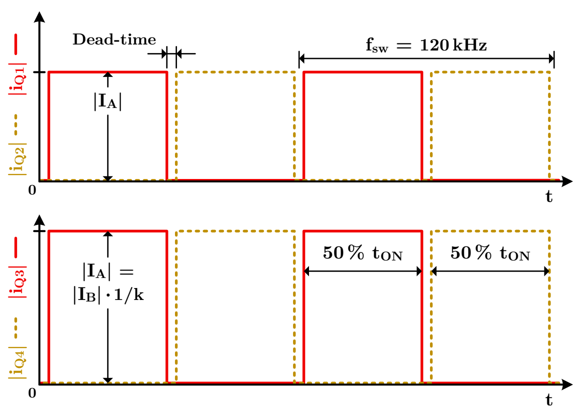
such a way that always one phase of transformer T1 is exactly active for 50 % of the period ($\gamma = 0.5$ and $\delta = 0.5$).[6] With a switching frequency f_{sw} of 120 kHz, this is a switch-on time of 4.167 µs per phase. The duty cycle of 50 % for all four switches (power MOSFETs) is independent of the currents and voltages in the circuit, as well as the energy flow direction of the converter. Therefore, no closed-loop control is required, neither for the primary nor for the secondary side. The voltages that occur on the primary and secondary side depend solely on the transfer ratio k respectively the turns ratio of T1 and are presented in idealized form in Figure 23. The WMPP77Q55-1u25 transformer specially designed for the battery management application has 7 turns on the primary side and 5 turns on the secondary side, resulting in a transfer ratio k of 0.714 29 (equation (2)). This transfer ratio can also be seen in the representation of the voltages (Figure 23) and currents (Figure 24). It should be noted here that the voltages at the MOSFETs (Q1, Q2, Q3 and Q4) are twice the supply voltage (U_{C2} and U_{C3}), since the same voltage is induced in the inactive phase as is applied in the active phase. The power MOSFETs used must withstand this voltage at any time.

Figure 23 – Push-pull converter - voltages



Source: by the author

Figure 24 – Push-pull converter - currents



Source: by the author

[6] A small dead-time of about 1 % is necessary to prevent a short circuit between the phases.

When the four MOSFETs are controlled with the fixed duty cycle ($\gamma = 0.5$ and $\delta = 0.5$), a state of equilibrium is established for the voltage U_{C2} and U_{C3} (e.g. 12.00 V and 8.57 V in Figure 19). The power consumed in this condition mainly covers the iron losses that result from the reversal of magnetization. However, if current is drawn from the output (I_B in Figure 22), the input side reacts to this in that the drawn current I_A also increases. As can be seen from equation (3), all currents are indirectly proportional to the ratio of the number of turns of the transformer. Since the primary and secondary sides are built up in the same way, this equation applies to both directions. Thus, a bidirectional energy transfer is possible without having to change the duty cycle. In case that the energy transfer takes place from the primary to the secondary side, the currents drawn in Figure 22 have a positive sign and Q3/Q4 work as a synchronous rectifier, while all currents are negative when the energy is transferred from the secondary to the primary side (Q1/Q2 take over the rectification function). Figure 24 therefore shows the magnitudes of the (idealized) currents. Due to the lack of a closed-loop control (fixed duty cycle of 0.5), the currents can have any high values, depending on the load. The transferable power is therefore only limited by the maximum operating temperature of the individual components.

$$k = \frac{n_{sec}}{n_{pri}} = \frac{u_{Q3}}{u_{Q1}} = \frac{u_{Q4}}{u_{Q2}} \approx \frac{U_{C3}}{U_{C2}} \tag{2}$$

$$k = \frac{n_{sec}}{n_{pri}} = \frac{i_{Q1}}{i_{Q3}} = \frac{i_{Q2}}{i_{Q4}} \approx \frac{I_A}{I_B} \tag{3}$$

When switching from one phase to the other, a small dead-time is necessary to avoid a short circuit between the two phases (Figure 23 and Figure 24). Since the transformer does not transmit any energy during this time, the two capacitors C2 and C3 have to absorb respectively deliver electrical energy for this short time. In addition, C2 and C3 stabilize the two voltage potentials **VZK** and *VZK* and decouple the push-pull converter from the input filter and the full-bridge circuit. This strict separation from the PI filter and the full-bridge allows the converter stage to be optimized independently of the other circuit parts, both in terms of f_{sw} and component selection.

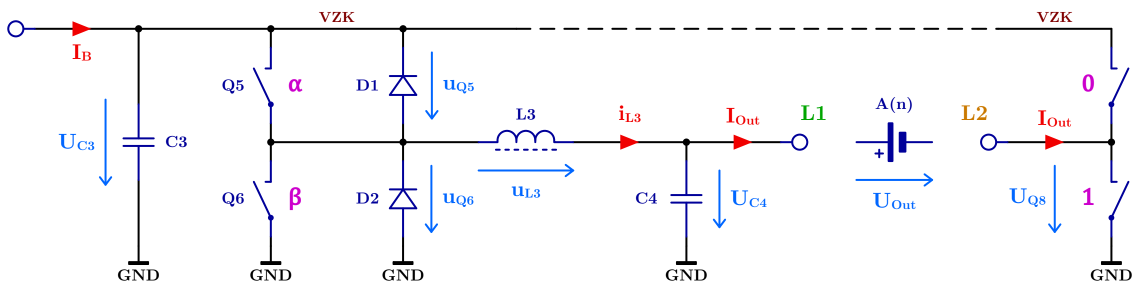
The fixed duty cycle of 50 % ($\gamma = 0.5$ and $\delta = 0.5$) enables a continuous energy transfer (no current peaks), so the transformer can be used optimally and the already good efficiency of a push-pull converter stage to be further increased. In addition, the power MOSFETs used also increase the efficiency, since MOSFETs have a much lower voltage drop than power diodes used in the original push-pull converter topology.

4.3.3 Full-Bridge Converter

The potential *VZK*, with a typical voltage of 8.57 V, differs strongly from the expected accumulator cell voltage (2.00 V to 4.50 V). For this reason, an extra energy converter stage is necessary to adapt both voltages to one another. In addition, the polarity of the output (*L1* and *L2* in Figure 19) must also be set, as the power multiplexer requires a positive or negative voltage depending on the internal switch positions (please refer subsection 4.3.2).

The DC/DC converter circuit uses a modified full-bridge stage (H-bridge) to implement these requirements. The basic circuit diagram of this full-bridge stage with currents and voltages drawn in is presented in Figure 25. As can be seen there, the right leg of the full-bridge consists of a conventional half-bridge, formed from the two power switches Q7 and Q8. The left leg, on the other hand, consists of a synchronous converter (C3, Q5, Q6, D1, D2, L3 and C4).[7] This structure not only allows to set voltage and current and their polarity (four quadrant operation), but also transfers energy in both directions so that the accumulator cell A(n) can be charged or discharged as required.

Figure 25 – Full-bridge structure - idealized



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In order to transmit electrical energy bidirectionally, the synchronous converter has a combined buck-boost function, during which the converter works either as a boost or a buck converter. A typical buck converter uses a power switch with a variable on/off time (duty cycle) and a flyback diode to control the flow of current in the storage choke. In Figure 25 this task will be done by switch Q5 and diode D2 to generate a lower output voltage (U_{C4}) from a higher input voltage (U_{C3}). With ideal switches (Q5 and D2) the two voltages U_{C3} and U_{C4} as well as the duty cycle α are only related via equation (4) where β is the time period during which diode D2 conducts the coil current i_{L3} ($\beta = 1 - \alpha$). This equation is also shown graphically as voltage-time areas in Figure 26 (blue $V \cdot s$ areas). It should be noted here that equation (4) only applies as long as continuous current mode (CCM) is guaranteed, in which the current in the inductance never approaches zero.

$$(U_{C3} - U_{C4}) \cdot \alpha = U_{C4} \cdot \beta \tag{4}$$

In the equilibrium state, which equation (4) specifies, on average no current flows through L3 ($I_{DC,L3} = 0$). Only when this equilibrium is slightly disturbed by taking current I_{Out} from C4 does a direct current $I_{DC,L3}$ add to the triangular ripple current, as shown in Figure 26 (I_{Out} corresponds to $I_{DC,L3}$ as well as I_{Cell}). In this case, the input current I_B

[7] The two diodes D1 and D2 briefly take over the current flow during the switching process (commutation process) and are implemented in parallel with the power MOSFETs on the printed circuit board.

reacts with an increase to be able to deliver the higher output power at C4. Since the in- and output power must be the same (ideal buck converter without losses), the currents are indirectly proportional to the voltages. Therefore, the relationship between currents, voltages and the duty cycle α can also be represented as

$$\alpha = \frac{U_{C4}}{U_{C3}} = \frac{I_B}{I_{Out}} . \tag{5}$$

Figure 26 – Buck converter mode

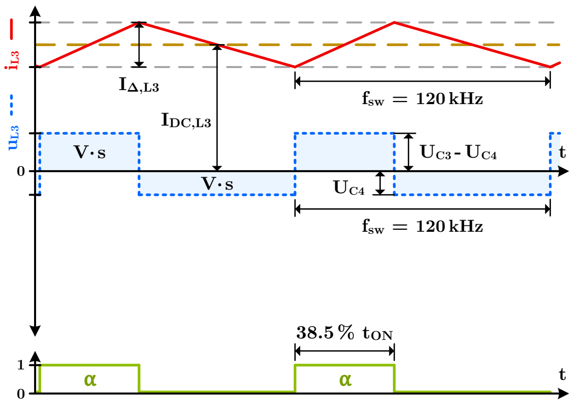

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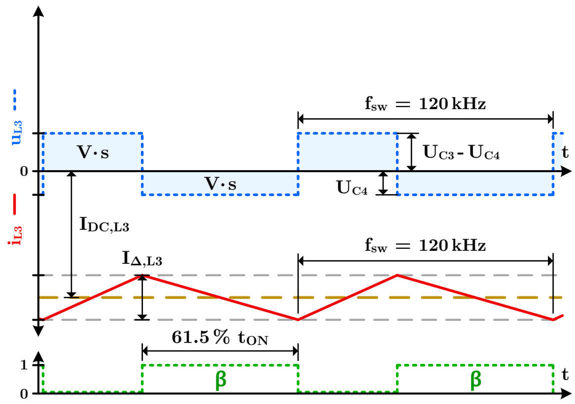
Figure 27 – Boost converter mode



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The circuit structure from Figure 25 can also operate like a boost converter by using the power switch Q6 and the flyback diode D1. In this case, energy is transferred from capacitor C4 to C3. For this purpose, Q6 must be controlled with the corresponding β duty cycle. Inductor current (i_{L3}) and voltage (u_{L3}) and the control signal β are shown in Figure 27, whereby the current i_{L3} is now negative because the direction of the power flow has reversed. Except for the negative current flow and the changed direction of energy flow, the curve shape of the buck and boost converters are very similar (Figure 26 and Figure 27). The equation (4) is therefore also valid for the boost converter.[8] In this case, α is the time during which the flyback diode D1 is conductive and energy is transferred to C3, while β controls the switch Q6. In addition, the voltages, currents and the control duty cycle β are related via the equation (6). If one considers that $\beta = 1 - \alpha$, this equation corresponds to equation (5).

$$\beta = 1 - \frac{U_{C4}}{U_{C3}} = 1 - \frac{I_B}{I_{Out}} \tag{6}$$

Since the same formulas apply to both the buck and the boost operation, there is no need to differentiate between these two operating modes and both power switches can be controlled with the α and β duty cycle at the same time (synchronous converter). Since both switches are switched on and off alternately (Figure 28), one of the switches is also active when the current has to flow through one of the flyback diodes and takes over the

[8] Only valid in continuous current mode (CCM).

current from this diode.[9] Due to the lower voltage drop of the switching elements (power MOSFETs), the losses are lower and the converter efficiency of the synchronous converter is higher compared to buck or boost converters, especially at low output voltages.

The two duty cycle control signals α and β of the synchronous converter are presented in Figure 28, whereby the duty cycle for α can vary between 0 % and 100 %. At which $\beta = 1 - \alpha$, β must be between 100 % and 0 % at the same time. Without a load (accumulator cell), this allows the voltage of U_{C4} to be set freely between zero and U_{C3} (*VZK* potential). With a voltage source (accumulator cell) on *L1* and *L2*, the duty cycle must be selected in such a way that equation (4) is always fulfilled. Any small deviation from this leads to a positive or negative equalizing current (I_{Out}). Theoretically, this current would rapidly become infinite. In reality, I_{Out} is limited by the unavoidable ohmic resistances in the circuit (not shown in Figure 25). To prevent destructive currents in the kA range, a fast closed-loop control for the current I_{Out} is absolutely necessary. Since $I_{DC,L3}$ is equal to I_{Out} (and I_{Cell}), this control also controls the current in the inductor L3 and, in combination with the cell voltage, the charge or discharge power for the accumulator cell. Thanks to the duty cycle, I_{Out} respectively $I_{DC,L3}$ can be set in a wide range, both positive and negative (Figure 28). Only the thermal heating and the saturation of the storage choke limit the current $I_{DC,L3}$.

Figure 28 – Synchronous converter mode

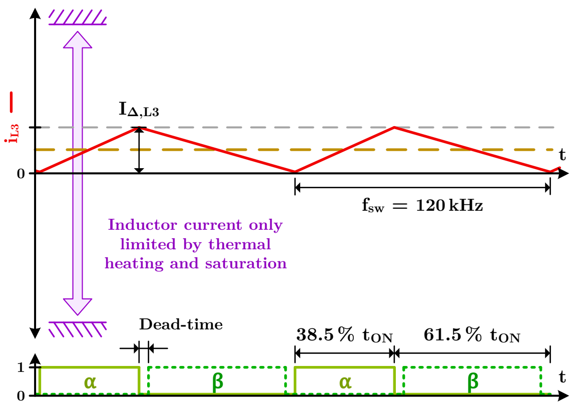

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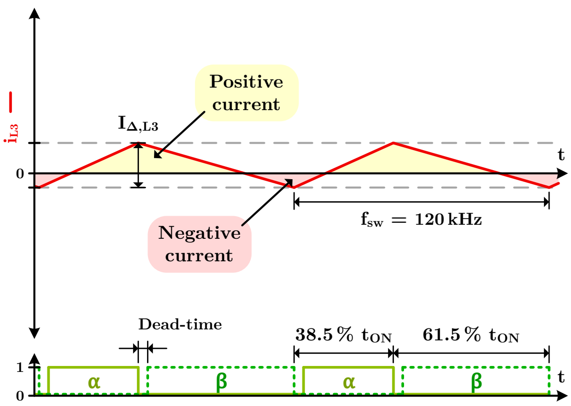
Figure 29 – Positive and negative currents



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Basically, there is no discontinuous current mode (DCM) for a synchronous converter. That means the current in the inductor never goes to zero and stays there. If the current $I_{DC,L3}$ is less than half the ripple current $I_{\Delta,L3}$, the inductor current i_{L3} will pass through the zero area but then continue to flow with the opposite sign. This condition is shown graphically in Figure 29. There, a part of the current is positive (yellow area) and a small part negative (red area). This means that i_{L3} flows mostly in the direction of capacitor C4, but then a small part back to C3. In the worst case, when $I_{Out} = 0$ ($I_{DC,L3} = 0$), the current only oscillates back and forth between capacitors C3 and C4. This current oscillation

9 A small dead-time of around 1 % is necessary between the α and β on-times to prevent a short circuit.

leads to slightly increased losses, especially with low cell charging and discharging currents. In contrast, the continuous current mode (CCM) of the synchronous converter allows a simplified closed-loop control, since equation (4) is always valid regardless of the I_{Out} current level and direction of flow.

A duty cycle of 38.5 % for α and 61.5 % for β are given in Figure 28 and Figure 29. At an input voltage of 8.57 V on C3, this results in a voltage of 3.3 V on C4. This 3.3 V is not necessarily applied to the accumulator cell, as the behavior of the half-bridge (right side in Figure 25) must also be considered. As can be seen from the circuit in Figure 25, either *GND* potential, *VZK* potential or a high-resistance state can be selected for *Line2* (*L2*) using the half-bridge. When the switch Q8 of the half-bridge is closed (Q7 open) and the *GND* potential is selected, the above-mentioned 3.3 V is applied to the accumulator cell. However, if switch Q7 is closed (Q8 open), there will be a negative −5.27 V for the accumulator cell (3.30 V − 8.57 V = −5.27 V). This negative voltage is required by the power multiplexer, depending on the internal switching status of the multiplexer (please refer subsection 4.3.2). Regardless of the sign, the voltage level from U_{Out} must be adjusted by changing the duty cycles. To get −3.3 V between *L1* and *L2* when switch Q7 is closed, the duty cycle α must be set to 61.5 % and β to 38.5 %.

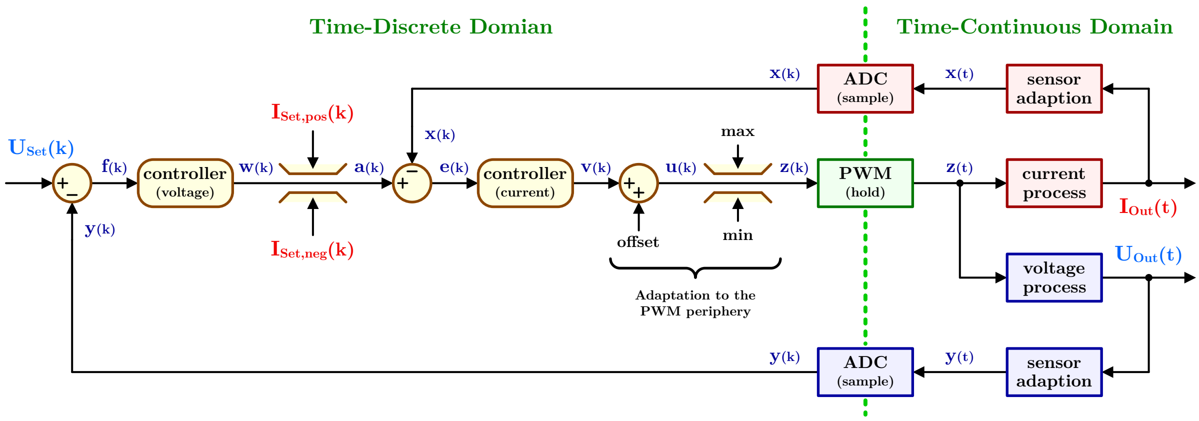
In terms of alternating current, the *VZK* potential is connected to C4 via the DC-link capacitor C3, so that the synchronous converter can be operated flawlessly even when switch Q7 is closed. In addition, point *L1* is connected to *VZK* via the accumulator cell in terms of alternating current. Although it can be assumed that the large capacity of the cell smooths the voltage at all times, the capacity C4 cannot be dispensed with. In combination with inductance L3, it acts as an output filter, so that only a negligible voltage and current ripple can occur on the connection cable of the battery stack. This minimizes the electromagnetic radiation on the cable. Furthermore, a minimum capacity at the output of the synchronous converter is necessary to be able to maintain a voltage regulation when no load is connected (accumulator cell is disconnected by the power multiplexer or the half-bridge circuit).

The magnitude of the ripple current $I_{\Delta,L3}$ depends on the voltage u_{L3}, the inductance L_{L3} of the storage choke and the switching frequency f_{sw}. For best results, this ripple current should be between 20 % and 30 % of the maximum rated current. With a frequency of 120 kHz and a storage inductance of 12.1 µH, as used by the prototype electronic, the result is a maximum $I_{\Delta,L3}$ of 2.03 A (please refer subsection 6.3.2). However, since the synchronous converter works independently of the push-pull converter stages, the frequency f_{sw} and the inductance of the storage choke L3 can be freely selected.

4.3.4 Closed-Loop Control Strategy

Although the push-pull converter works without regulation, a closed-loop control is essential for the operation of the synchronous converter used. The closed-loop control not only influences the energy with which the accumulator cell is charged or discharged, but also indirectly determines the power that has to be transmitted via the input PI filter, the push-pull converter and the power multiplexer. Since the polarity of the voltage U_{Out} can be positive as well as negative and the cell should be charged and discharged (I_{Out}), a four-quadrant closed-loop control is necessary. Based on the measured signals, the control algorithm, implemented in the microcontroller, must generate the two duty cycle signals α and β for the synchronous converter in real time. A simplified schematic representation of the digital closed-loop control principle as it is used in the prototype battery management system is shown in Figure 30.

Figure 30 – Simplified closed-loop control structure



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As a feedback signal for the closed-loop control, at least the voltage U_{Out} and the balancing current I_{Out} are used (Figure 30).[10] U_{Out} and I_{Out} are taken directly from the output of the full-bridge, as shown in Figure 19, whereby the sign of the measurement signal can be positive or negative (four-quadrant operation - please refer Table 3). The measured value of these two signals is low-pass filtered and adapted for the analog-digital converter (ADC). After digitization, the signals are made available to the closed-loop control algorithm (Figure 30). The result of the algorithm is written to the PWM peripheral module and specifies there the duty cycle α and β. The electrical behavior of the power stages (see transfer function in chapter 5) are indicated in Figure 30 with the voltage and current process blocks. These two blocks, in combination with the sensor adaptation, ultimately determine the necessary controller structure (e.g. PID controller) and its coefficients. Since the currently implemented controllers and especially the coefficients are not fully optimized and tested, these values are not given here. Regardless of this, the proposed controller structure is sufficient to carry out initial tests with the hardware.

[10] Other measured values such as the DC-link voltage and temperature can also be considered.

Table 3 – Four-quadrant operating states of the closed-loop control

Quad.	Cell operating state	Full-bridge converter settings	Feedback signal
1	charge selected cell positive pole on *Line1* (negative on *L2*)	close power switch Q8 (Q7 open) set positive setpoint value at U_{Set} set current limitation with $I_{Set,pos}$	U_{Out} is positive I_{Out} is positive
2	discharge selected cell positive pole on *Line1*	close power switch Q8 (Q7 open) set positive setpoint value at U_{Set} set current limitation with $I_{Set,neg}$	U_{Out} is positive I_{Out} is negative
3	charge selected cell negative pole on *Line1*	close power switch Q7 (Q8 open) set negative setpoint value at U_{Set} set current limitation with $I_{Set,neg}$	U_{Out} is negative I_{Out} is negative
4	discharge selected cell negative pole on *Line1*	close power switch Q7 (Q8 open) set negative setpoint value at U_{Set} set current limitation with $I_{Set,pos}$	U_{Out} is negative I_{Out} is positive

Source: by the author

The entire structure from Figure 30 results in a cascade closed-loop control with an inner current regulator and an outer voltage regulator, which works in all four quadrants as indicated in Table 3. In the controller structure shown, it should be emphasized that three setpoints are used. U_{Set} specifies the target voltage that the accumulator cell should have at the end of the balancing process. Depending on the switch position of the power multiplexer, this setpoint must have an appropriate sign to generate a positive or negative output voltage. $I_{Set,pos}$ and $I_{Set,neg}$ define the maximum balancing current with which the accumulator cell is to be charged or discharged. If the cell voltage U_{Cell} approaches the setpoint value U_{Set}, the balancing current I_{Out} (I_{Cell}) is automatically reduced until it reaches zero. In this case, the control algorithm works as a constant current constant voltage charge controller (CC-CV charger), both during charging and discharging the accumulator cell. However, since U_{Set}, $I_{Set,pos}$ and $I_{Set,neg}$ can be freely selected, every charging/discharging strategy can be implemented by adapting these setpoints during the balancing process.

The charge/discharge current of the accumulator cell (I_{Cell} respectively I_{Out}) causes a voltage drop both on the power multiplexer and on the connection cable of the battery stack (balancing cable). In this case, the voltage measured at points *L1* and *L2* may not match the real cell voltage ($U_{Out} \neq U_{Cell}$). In order to still be able to determine the cell voltage with high accuracy, the full bridge must be deactivated so that I_{Cell} (I_{Out}) becomes zero. This interruption of the balancing process should take place periodically (e.g. every 10 seconds) to continuously monitor the condition of the accumulator cell and to adjust the charging/discharging process if necessary.

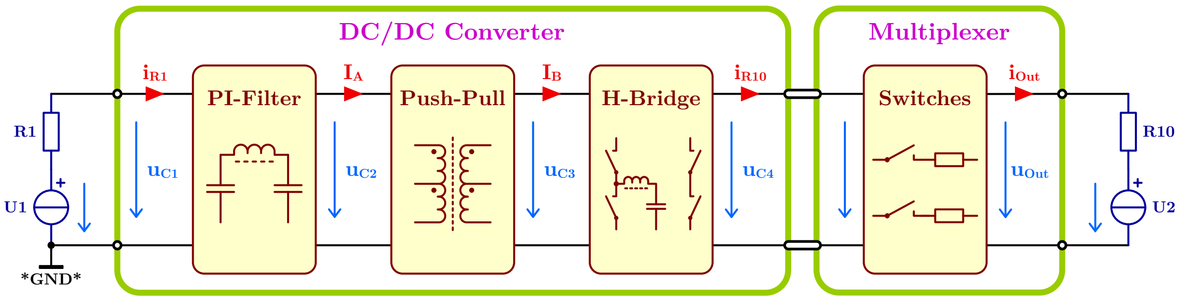
5 MATHEMATICAL MODEL

The previous description of the battery management system considers the components as ideal elements and neglects their typical ohmic part. In addition, for the reason of clarity, the leakage inductance of the transformer and the auxiliary power supplies on the primary and secondary sides were not mentioned. However, these elements are required for a complete description of the overall system. From this, a mathematical model can be created, which describes the interaction of the individual energy converter stages, the accumulator cell to be balanced and the 12 V auxiliary power supply. The mathematical model allows the closed-loop control and its parameters to be optimally designed and further investigations (stability analysis, efficiency assessment, component optimization, etc.) to be carried out.[1]

5.1 Replacement Circuit Modeling

As before, the entire electronic for the mathematical model is divided into two parts, as shown in Figure 31. The description of the multiplexer function as a mathematical model turns out to be simple. Basically, the energy to charge respectively discharge the selected accumulator cell always flows over two power switches (continually on) and their associated resistance. This bidirectional semiconductor switches are in series to the resistance of the output cable and the accumulator cell U2 in Figure 31 and can be therefore combined to form one common resistor R10. The supply for controlling the bidirectional power switches is provided by the DC/DC converter unit and counted there as part of the secondary side housekeeping supply. Therefore, resistor R10 alone, with a resistance of approximately 70 mΩ, is sufficient as a replacement circuit for the multiplexer and the connection cable.

Figure 31 – Simple block diagram of the power stages



Source: by the author

More complex is the mathematical model for the DC/DC converter unit. This printed circuit board module is a fully embedded, high integrated, two stage energy converter with

1 No longer part of this work.

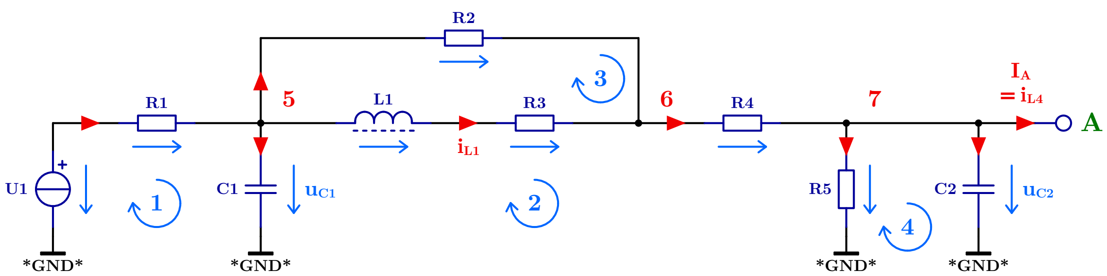
potential separation, which allows transferring energy in both directions (bidirectional). A precise simulation model for the whole circuit is impossible, but for the power flow path a replacement circuit can be modelled. Therefore, the circuit is divided into three parts (left side in Figure 31). The input PI filter (Figure 32), the push-pull converter (Figure 33) and the full-bridge stage with an integrated synchronous converter (Figure 34 respectively Figure 36).

To reduce the mathematical complexity, only the leakage inductance of the transformer, the copper resistance of the inductors/transformer and the switch-on resistance of the power switches are modelled. The equivalent series resistance (ESR) of the capacitors is ignored (several ceramic capacitors are used in parallel to archive low ESR and ESL). The housekeeping supplies for the primary and secondary side are modelled by two resistors (R5 and R8). The battery management electronic (and the mathematical model) will not work without the two power supplies U1 and U2 in Figure 31. While U2 represents the accumulator cell to be balanced, U1 provides the energy required for operation (12 V auxiliary power supply). Hence, the energy transfer is bidirectional, both sources must have charge and discharge capability (accumulators).

5.1.1 PI Filter Input Stage

In order to attenuate noise and electromagnetic radiation caused by the high-frequency switching of the power stages, a PI filter is required at the input. Figure 32 shows the circuit of this input stage, whereby the illustrated components are described in Table 4. The replacement circuit also includes the 12 V auxiliary power supply (U1) and the resistance of the connection cable with an assumed length of 2.0 m (R1).

Figure 32 – PI filter replacement circuit



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Thanks to Kirchhoff's current and voltage law (Küpfmüller; Mathis; Reibiger, 2008), seven formulas for the meshes and nodes of the circuit in Figure 32 can be determined (equation (7) until (13)). These formulas can then be reduced to the three differential equations (14), (15) and (16) that describes the voltage and current changes in the three energy storage elements C1, L1 and C2.

Table 4 – PI filter replacement circuit - element description

U1	12 V auxiliary supply with charge and discharge capability	$U_{U1} = 12.00\,\mathrm{V}$
R1	resistance of connection cable - 1.5 mm^2, 2.0 m long	$R_{R1} = 46.78\,\mathrm{m\Omega}$
C1	input capacitor - ceramic capacitors connected in parallel	$C_{C1} = 20.00\,\mathrm{\mu F}$
R2	damping resistor to reduce oscillation in the filter	$R_{R2} = 2.20\,\Omega$
L1	wire-wound power inductor with ferrite core	$L_{L1} = 1.80\,\mathrm{\mu H}$
R3	copper resistance of the wire-wound power inductor L1	$R_{R3} = 3.00\,\mathrm{m\Omega}$
R4	15 A, 5 mΩ safety fuse - to prohibit cable fire	$R_{R4} = 5.00\,\mathrm{m\Omega}$
R5	auxiliary power supply on the primary side of the converter	$R_{R5} = 850.00\,\Omega$
C2	DC-link capacitor - electrolytic and ceramic in parallel	$C_{C2} = 134.40\,\mathrm{\mu F}$

Source: by the author

$$\text{1} \qquad 0 = -u_{U1} + u_{R1} + u_{C1} \tag{7}$$

$$\text{2} \qquad 0 = -u_{C1} + u_{L1} + u_{R3} + u_{R4} + u_{R5} \tag{8}$$

$$\text{3} \qquad 0 = u_{R2} - u_{R3} - u_{L1} \tag{9}$$

$$\text{4} \qquad 0 = u_{C2} - u_{R5} \tag{10}$$

$$\text{5} \qquad 0 = i_{R1} - i_{C1} - i_{L1} - i_{R2} \tag{11}$$

$$\text{6} \qquad 0 = i_{R2} + i_{L1} - i_{R4} \tag{12}$$

$$\text{7} \qquad 0 = i_{R4} - i_{R5} - i_{C2} - I_A \tag{13}$$

$$C_{C1} \cdot \frac{\mathrm{d}u_{C1}}{\mathrm{d}t} = -u_{C1} \cdot \frac{R_{R1} + R_{R2} + R_{R4}}{R_{R1} \cdot (R_{R2} + R_{R4})} - i_{L1} \cdot \frac{R_{R2}}{R_{R2} + R_{R4}} + u_{C2} \cdot \frac{1}{R_{R2} + R_{R4}} + u_{U1} \cdot \frac{1}{R_{R1}} \tag{14}$$

$$L_{L1} \cdot \frac{\mathrm{d}i_{L1}}{\mathrm{d}t} = u_{C1} \cdot \frac{R_{R2}}{R_{R2} + R_{R4}} - i_{L1} \cdot \frac{R_{R2}\, R_{R3} + R_{R2}\, R_{R4} + R_{R3}\, R_{R4}}{R_{R2} + R_{R4}} - u_{C2} \cdot \frac{R_{R2}}{R_{R2} + R_{R4}} \tag{15}$$

$$C_{C2} \cdot \frac{\mathrm{d}u_{C2}}{\mathrm{d}t} = u_{C1} \cdot \frac{1}{R_{R2} + R_{R4}} + i_{L1} \cdot \frac{R_{R2}}{R_{R2} + R_{R4}} - u_{C2} \cdot \frac{R_{R2} + R_{R4} + R_{R5}}{R_{R5} \cdot (R_{R2} + R_{R4})} - I_A \tag{16}$$

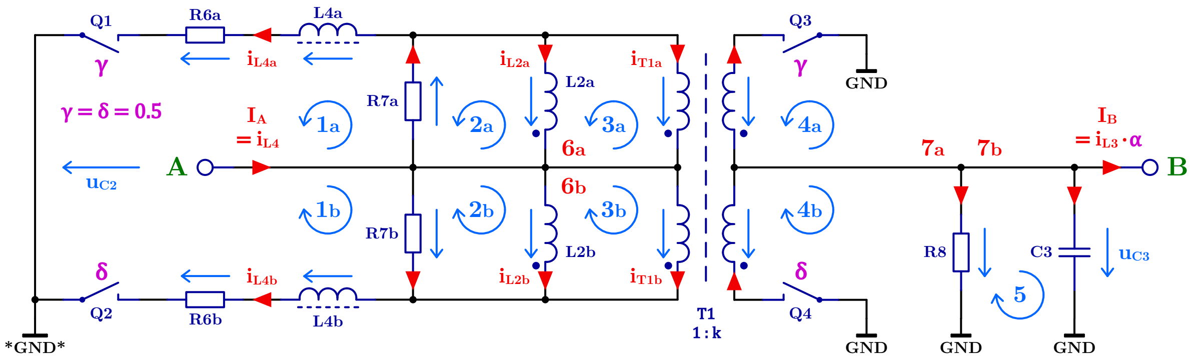
5.1.2 Push-Pull Converter Stage

By reason of the different voltage levels between input and output of the battery management system, an electrical potential separation is essential. This is the task of the push-pull converter stage (Schlienz, 2007), whose equivalent circuit is shown in Figure 33 and their elements are described in Table 5. Thereby, the secondary switches Q3 and Q4 replaces the typical diodes and work as a synchronous rectifier.[2] To avoid saturation of the transformer core, the two phases and their elements must be completely symmetrical.

[2] This also allows a bidirectional energy transfer.

That means, R6a and R6b, L4a and L4b, R7a and R7b as well as L2a and L2b must have the same values (deviation $< 0.5\,\%$). This is achieved through a symmetrical structure of the transformer, the same switch parameters for Q1/Q2 and Q3/Q4 and an equal duty cycle of $50\,\%$ for both phases ($\gamma = 0.5$ and $\delta = 0.5$).

Figure 33 – Push-pull converter replacement circuit



Source: by the author

Table 5 – Push-pull converter replacement circuit - element description

R6	series connection of DC resistance as stated:	$R_{R6} = 32.39\,\mathrm{m\Omega}$
	copper resistance of transformer: $R_{pri} = 12.85\,\mathrm{m\Omega}$	
	copper resistance of transformer: $1/k^2 \cdot R_{sec} = 11.53\,\mathrm{m\Omega}$	
	on resistance of switch Q1/Q2: $R_{DSon} = 3.30\,\mathrm{m\Omega}$	
	on resistance of switch Q3/Q4: $1/k^2 \cdot R_{DSon} = 4.70\,\mathrm{m\Omega}$	
L4	leakage (stray) inductance of the push-pull transformer	$L_{L4} = 241.00\,\mathrm{nH}$
R7	core loss of N97 ferrite - EFD20, 115 mT, 120 kHz	$R_{R7} = 750.00\,\Omega$
L2	main inductance of the EFD20 N97 push-pull transformer	$L_{L2} = 61.25\,\mathrm{\mu H}$
T1	ideal transformer with transfer ratio of $1 : k$	
1:k	turn ratio of the transformer: $k = n_{sec}/n_{pri} = 5/7 = 1/1.4$	$k = 714.29\,\mathrm{m}$
R8	auxiliary power supply on the secondary side of the converter	$R_{R8} = 100.00\,\Omega$
C3	DC-link capacitor - electrolytic and ceramic in parallel	$C_{C3} = 376.20\,\mathrm{\mu F}$

Source: by the author

Although phase A and phase B are completely symmetrical, they must be considered separately to create a mathematical model. The reason for this is the transformer used. Since all windings (L2a, L2b and the windings of the ideal transformer T1) are applied to a common core and are thus magnetically coupled, all voltage vectors must point to the beginning of the windings (points at the coils), as shown in Figure 33. This does not apply to the leakage inductances L4a and L4b, as these are not magnetically coupled to the other coils.

By using Kirchhoff's laws for phase A, the formulas (17) until (23) can be determined and for phase B the formulas (24) until (30) are valid. Since the values of the resistors and inductors from phase A and B are equal ($R_{R6a} = R_{R6b} = R_{R6}$ and so on), the formulas are very similar and only differ in the sign of some individual terms.

$$\text{1a} \quad 0 = -u_{C2} + u_{R7a} + u_{L4a} + u_{R6a} \tag{17}$$
$$\text{2a} \quad 0 = -u_{R7a} - u_{L2a} \tag{18}$$
$$\text{3a} \quad 0 = u_{L2a} - u_{T1a} \tag{19}$$
$$\text{4a} \quad 0 = u_{T1a} \cdot k + u_{R8} \tag{20}$$
$$\text{5a} \quad 0 = -u_{R8} + u_{C3} \tag{21}$$
$$\text{6a} \quad 0 = I_A - i_{R7a} + i_{L2a} + i_{T1a} \tag{22}$$
$$\text{7a} \quad 0 = -i_{T1a} \cdot 1/k - i_{R8} - i_{C3} - I_B \tag{23}$$

$$\text{1b} \quad 0 = -u_{C2} + u_{R7b} + u_{L4b} + u_{R6b} \tag{24}$$
$$\text{2b} \quad 0 = -u_{R7b} + u_{L2b} \tag{25}$$
$$\text{3b} \quad 0 = -u_{L2b} + u_{T1b} \tag{26}$$
$$\text{4b} \quad 0 = -u_{T1b} \cdot k + u_{R8} \tag{27}$$
$$\text{5b} \quad 0 = -u_{R8} + u_{C3} \tag{28}$$
$$\text{6b} \quad 0 = I_A - i_{R7b} - i_{L2b} - i_{T1b} \tag{29}$$
$$\text{7b} \quad 0 = i_{T1b} \cdot 1/k - i_{R8} - i_{C3} - I_B \tag{30}$$

If one considers that phase A and B are each active 50 % of the period time, three differential equations for the energy storage elements L4, L2 and C3 can be derived from the previous formulas. The value of equation (32) is always zero, since the individual terms of L2 for phase A and B cancel each other out. This means that the energy in the main inductance L2 from one period to the next period does not change.[3] L2 also does not appear in the differential equation (31) and (33), so that the main inductance L2 of the transformer T1 is unnecessary for the mathematical model of the converter and can be omitted. Thus, the two differential equations (31) and (33) are sufficient to fully describe the push-pull converter stage.

$$L_{L4} \cdot \frac{\mathrm{d}i_{L4}}{\mathrm{d}t} = u_{C2} - I_A \cdot R_{R6} - u_{C3} \cdot \frac{1}{k} \tag{31}$$

$$L_{L2} \cdot \frac{\mathrm{d}i_{L2}}{\mathrm{d}t} = 0 \tag{32}$$

$$C_{C3} \cdot \frac{\mathrm{d}u_{C3}}{\mathrm{d}t} = I_A \cdot \frac{1}{k} - u_{C3} \cdot \frac{R_{R7} \cdot k^2 + R_{R8}}{R_{R7} \cdot R_{R8} \cdot k^2} - I_B \tag{33}$$

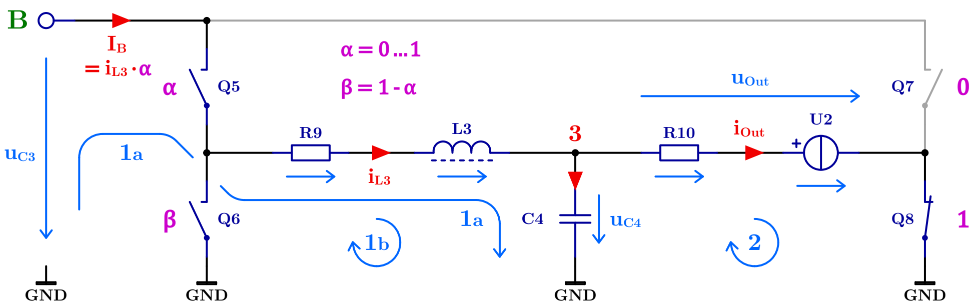
5.1.3 Full-Bridge Converter Stage

The third stage in the power flow path is a full-bridge circuit illustrated in Figure 34 (corresponding component description are given in Table 6). On the left leg of the full-bridge, the switches Q5/Q6 with R9, L3 and C4 form a synchronous converter (Schlienz,

[3] However, within a cycle (period), energy is absorbed by the inductance and emitted again.

2007) that can transfer energy in both directions (buck or boost mode). To transfer energy bidirectionally, two power sources with charging and discharging capability must be available (U1 and U2 in Figure 31). In this case, an energy transfer and its direction depends solely on the duty cycles of α and β ($\beta = 1 - \alpha$) and the voltages of the two sources. In other words, the synchronous converter generates a selectable voltage u_{C4} between zero and u_{C3} by selecting a duty cycle between 0 % and 100 %.[4] The current direction and amplitude (and consequently the transferred power) depends only on the imbalance between u_{C4} and u_{U2} ($i_{Out} = (u_{C4} - u_{U2})/R_{R10}$).[5]

Figure 34 – Full-bridge stage replacement circuit - switch Q8 closed



Source: by the author

Table 6 – Full-bridge stage replacement circuit - element description

R9	series connection of DC resistance as stated:	$R_{R9} =$	9.53 mΩ
	on resistance of switch Q5/Q6: $R_{DSon} = 2.40\,\mathrm{m\Omega}$		
	copper resistance of power inductor L3: $R_{L3} = 7.13\,\mathrm{m\Omega}$		
L3	power inductor - EFD20 with 0.49 mm air gap, N87 material	$L_{L3} =$	12.10 µH
C4	output capacitor - ceramic capacitors connected in parallel	$C_{C4} =$	70.40 µF
R10	series connection of DC resistance as stated:	$R_{R10} =$	70.53 mΩ
	4 mΩ shunt resistor to measure the output current i_{Out}		
	20 A, 3 mΩ safety fuse - to prohibit cable fire		
	power-multiplexer - two power switches: $2 \cdot 22.50\,\mathrm{m\Omega}$		
	connection cable resistance - $1.0\,\mathrm{mm}^2$, $2 \cdot 0.5\,\mathrm{m}$: 17.54 mΩ		
	on resistance of switch Q8/Q7: $R_{DSon} = 1.00\,\mathrm{m\Omega}$		
U2	3.3 V accumulator cell with charge and discharge capability	$U_{U2} =$	3.30 V

Source: by the author

The synchronous converter enables individual charging or discharging of an accumulator cell (U2) by varying the duty cycle. Since the synchronous converter does not have a discontinuous current mode (DCM), the current in the inductor L3 can reverse the direction at light load respectively low currents during a switching period. As a result, the power losses increase slightly compared to buck/boost topologies with diodes. In contrast to

[4] u_{C3} corresponds to the *VZK* potential.
[5] The given formula only applies when switch Q7 is open and switch Q8 is closed.

this, the continuous current mode (CCM) of the converter guarantees a linear relationship between the duty cycle and the voltages u_{C3} and u_{C4} at all time, which considerably simplifies the control.

Depending on the selected accumulator cell and the corresponding switch status of the multiplexer, the voltage of U2 can be positive or negative. In order to be able to generate a positive or negative voltage for u_{U2}, the right connection point of the voltage source U2 (accumulator cell) can be switched to 0 V (Figure 34) or to u_{C3} (please refer subsection 5.3.1). Therefore, the switches Q7 and Q8 forms a half-bridge circuit (right leg in Figure 34), in which the switches are controlled statically. To select a new accumulator cell using the power multiplexer, all four switches (Q5 until Q8) must be deactivated. After selecting the desired cell, Q7 or Q8 is switched on (depending on the cell polarity) and then the synchronous converter (Q5 and Q6) can be restarted and the closed-loop control will set the required voltage respectively current.

The replacement circuit from Figure 34 can also be analyzed by Kirchhoff's laws. There are two meshes and one node who will give three formulas. But by switching Q5 and Q6 alternately, the mesh 1 changes constantly and two modes during one switching period exists. So four formulas are necessary to describe the system (Erickson; Maksimović, 2004).

$$\text{1a} \qquad 0 = -u_{C3} + u_{R9} + u_{L3} + u_{C4} \tag{34}$$
$$\text{1b} \qquad 0 = u_{R9} + u_{L3} + u_{C4} \tag{35}$$
$$\text{2} \qquad 0 = -u_{C4} + u_{R10} + u_{U2} \tag{36}$$
$$\text{3} \qquad 0 = i_{L3} - i_{C4} - i_{R10} \tag{37}$$

The difference between the two formulas (34) and (35) is only the $-u_{C3}$ term and this part is only active during the α on-time (switch Q5 is closed). During the β on-time ($\beta = 1 - \alpha$) switch Q6 only closes the loop and adds 0 V to the mesh. Therefore, β will not appear in the formulas. The four formulas can now be reduced to form the two differential equations (38) and (39), which describe the voltage and current changes in the two energy storage elements L3 and C4.

$$L_{L3} \cdot \frac{\mathrm{d}i_{L3}}{\mathrm{d}t} = u_{C3} \cdot \alpha - i_{L3} \cdot R_{R9} - u_{C4} \tag{38}$$

$$C_{C4} \cdot \frac{\mathrm{d}u_{C4}}{\mathrm{d}t} = i_{L3} - u_{C4} \cdot \frac{1}{R_{R10}} + u_{U2} \cdot \frac{1}{R_{R10}} \tag{39}$$

5.2 State-Space Representation

The seven differential equations found (equation (14), (15), (16), (31), (33), (38) and (39)) can now be clearly described as a state-space representation (Erickson; Maksimović, 2004; Horn; Dourdoumas, 2004) in the form

$$\mathbf{K} \cdot \frac{\mathrm{d}\mathbf{x}(t)}{\mathrm{d}t} = \mathbf{A} \cdot \mathbf{x}(t) + \mathbf{B} \cdot \mathbf{u}(t)\,, \tag{40}$$

$$\mathbf{y}(t) = \mathbf{C} \cdot \mathbf{x}(t) + \mathbf{D} \cdot \mathbf{u}(t)\,. \tag{41}$$

However, before the equations can be brought into matrix form, a mathematical connection among the three replacement circuits must be made. These are the four terms u_{C2}, I_A, u_{C3} and I_B. While u_{C2} and u_{C3} are already known, two formulas for I_A and I_B are necessary. These formulas can be easily determined from Figure 33 and Figure 34 and are

$$I_A = i_{L4}\,, \qquad\qquad I_B = i_{L3} \cdot \alpha\,. \tag{42}$$

The equations for the output vector $\mathbf{y}(t)$ must also be defined and depend on which values are to be considered. In our case, the most important value is i_{Out} (equal to i_{R10}). This current is used by the closed-loop control to regulate the entire system, charges respectively discharges the accumulator cell (U2) and shows also the energy flow direction.

The second interesting value is the voltage u_{Out} on the elements R10 and U2 in Figure 34. If no load is available (no U2 source exists) or the actual current is lower than the current set-point value, the closed-loop control will regulate this u_{Out} voltage. This condition can be modelled by choosing $R_{R10} = 100\,\mathrm{k\Omega}$ (light load condition). For this purpose, the electronic measures the difference voltage on the full-bridge output (Q8 closed: $u_{Out} = u_{C4} - 0\,\mathrm{V}$; Q7 closed: $u_{Out} = u_{C4} - u_{C3}$). If the synchronous converter is disabled and no voltage drop on R10 occurs, this voltage also corresponds to the accumulator cell voltage. The corresponding equations for the $\mathbf{y}(t)$-vector are presented in equation (43) and (44).[6]

$$i_{Out} = u_{C4} \cdot \frac{1}{R_{R10}} - u_{U2} \cdot \frac{1}{R_{R10}} \tag{43}$$

$$u_{Out} = u_{C4} \tag{44}$$

Summarized, all the given equations results in a complete mathematical model for the block diagram in Figure 31. This state-space representation is shown in equation (50) and (51), where the term $(\mathbf{A_1} - \mathbf{A_2}) \cdot \mathbf{X}$ must be set to zero.[7]

5.2.1 Small-Signal AC Model

In the state-space representation, the α duty cycle is a constant value and does not change over time. For a closed-loop control, which continuously adjust α, a dynamic model is necessary (Erickson; Maksimović, 2004). This small-signal AC model describes how small variations of the U1 and U2 sources and the α duty cycle will change the outputs i_{Out} and u_{Out}. Therefore, the linearized AC model (non-linear terms are ignored) is

[6] Only $u_{Out} = u_{C4} - 0\,\mathrm{V}$ -mode with Q8 is closed is shown.
[7] $(\mathbf{A_1} - \mathbf{A_2}) \cdot \mathbf{X}$ is only required for the small-signal AC model (subsection 5.2.1).

$$\mathbf{K}\cdot\frac{\mathrm{d}\mathbf{x}(t)}{\mathrm{d}t}=\mathbf{A}\cdot\mathbf{x}(t)+\mathbf{B}\cdot\mathbf{u}(t)+\Big\{(\mathbf{A_1}-\mathbf{A_2})\cdot\mathbf{X}+(\mathbf{B_1}-\mathbf{B_2})\cdot\mathbf{U}\Big\}\cdot\alpha(t)\,, \tag{45}$$

$$\mathbf{y}(t)=\mathbf{C}\cdot\mathbf{x}(t)+\mathbf{D}\cdot\mathbf{u}(t)+\Big\{(\mathbf{C_1}-\mathbf{C_2})\cdot\mathbf{X}+(\mathbf{D_1}-\mathbf{D_2})\cdot\mathbf{U}\Big\}\cdot\alpha(t)\,. \tag{46}$$

The matrices $\mathbf{A_1}$, $\mathbf{B_1}$, $\mathbf{C_1}$ and $\mathbf{D_1}$ are "mode-1" matrices with those elements are active when switch Q5 is closed (Q6 opened), while matrices $\mathbf{A_2}$, $\mathbf{B_2}$, $\mathbf{C_2}$ and $\mathbf{D_2}$ are "mode-2" matrices with those elements are active when switch Q6 is closed (Q5 opened). In matrix $\mathbf{B}$, $\mathbf{C}$ and $\mathbf{D}$ every term is active during all time of the period and consequently during the mode-1 and mode-2 time also, therefore the subtraction of the individual matrix results in zero. Only the matrix $\mathbf{A}$ has two terms who differ between mode-1 and mode-2 (terms with α inside). Thus, $\mathbf{A_1}-\mathbf{A_2}$ for the AC model is

$$\mathbf{A_1}-\mathbf{A_2}=\begin{bmatrix}0&0&0&0&0&0&0\\0&0&0&0&0&0&0\\0&0&0&0&0&0&0\\0&0&0&0&0&0&0\\0&0&0&0&0&-1&0\\0&0&0&0&1&0&0\\0&0&0&0&0&0&0\end{bmatrix}. \tag{47}$$

In equation (45) the $\mathbf{A_1}-\mathbf{A_2}$ is multiplied with an unknown vector $\mathbf{X}$. This vector is now to be determined. For this, the state-space representation in equilibrium (Erickson; Maksimović, 2004), where all derivatives are zero, is used ($\mathbf{0}=\mathbf{A}\cdot\mathbf{X}+\mathbf{B}\cdot\mathbf{U}$). Rearranging will give

$$\mathbf{X}=-\mathbf{A}^{-1}\cdot\mathbf{B}\cdot\mathbf{U}\,. \tag{48}$$

If the corresponding terms from equation (50) are used in equation (48), a vector with seven elements results. Due to the size of the matrix $\mathbf{A}$ and its inversion, individual terms can form huge expressions. In our case, where the first to the fourth columns as well as column seven of the matrix $\mathbf{A_1}-\mathbf{A_2}$ are full of zeros, the $(\mathbf{A_1}-\mathbf{A_2})\cdot\mathbf{X}$ vector will have only two big terms with values on position five and six. This vector is shown in equation (49) where an ### symbol replaces the appropriate big expressions.[8] By adding this vector to the state-space representation (please refer equation (50) and (51)) a small-signal AC model for the DC/DC converter can be specified.

$$(\mathbf{A_1}-\mathbf{A_2})\cdot\mathbf{X}=\begin{bmatrix}0&0&0&0&\#\#\#&\#\#\#&0\end{bmatrix}^T \tag{49}$$

[8] Inserting the values given in the tables results in $(\mathbf{A_1}-\mathbf{A_2})\cdot\mathbf{X}=\begin{bmatrix}0&0&0&0&0.0238&8.5665&0\end{bmatrix}^T$ for $R_{R10}=70.53\,\mathrm{m\Omega}$ and $(\mathbf{A_1}-\mathbf{A_2})\cdot\mathbf{X}=\begin{bmatrix}0&0&0&0&0.0000&8.5661&0\end{bmatrix}^T$ for $R_{R10}=100\,\mathrm{k\Omega}$.

$$
\begin{bmatrix} C_{C1} \cdot \frac{\mathrm{d}u_{C1}}{\mathrm{d}t} \\ L_{L1} \cdot \frac{\mathrm{d}i_{L1}}{\mathrm{d}t} \\ C_{C2} \cdot \frac{\mathrm{d}u_{C2}}{\mathrm{d}t} \\ L_{L4} \cdot \frac{\mathrm{d}i_{L4}}{\mathrm{d}t} \\ C_{C3} \cdot \frac{\mathrm{d}u_{C3}}{\mathrm{d}t} \\ L_{L3} \cdot \frac{\mathrm{d}i_{L3}}{\mathrm{d}t} \\ C_{C4} \cdot \frac{\mathrm{d}u_{C4}}{\mathrm{d}t} \end{bmatrix} = \begin{bmatrix} -\frac{R_{R1}+R_{R2}+R_{R4}}{R_{R1}\cdot(R_{R2}+R_{R4})} & -\frac{R_{R2}}{R_{R2}+R_{R4}} & \frac{1}{R_{R2}+R_{R4}} & 0 & 0 & 0 & 0 \\ \frac{R_{R2}}{R_{R2}+R_{R4}} & -\frac{R_{R2}\cdot R_{R3}+R_{R2}\cdot R_{R4}+R_{R3}\cdot R_{R4}}{R_{R2}+R_{R4}} & -\frac{R_{R2}}{R_{R2}+R_{R4}} & 0 & 0 & 0 & 0 \\ \frac{1}{R_{R2}+R_{R4}} & \frac{R_{R2}}{R_{R2}+R_{R4}} & -\frac{R_{R2}+R_{R4}+R_{R5}}{R_{R5}\cdot(R_{R2}+R_{R4})} & -1 & 0 & 0 & 0 \\ 0 & 0 & 1 & -R_{R6} & -\frac{1}{k} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{k} & -\frac{R_{R7}\cdot k^2+R_{R8}}{R_{R7}\cdot R_{R8}\cdot k^2} & -\alpha & 0 \\ 0 & 0 & 0 & 0 & \alpha & -R_{R9} & -1 \\ 0 & 0 & 0 & 0 & 0 & 1 & -\frac{1}{R_{R10}} \end{bmatrix} \cdot \begin{bmatrix} u_{C1} \\ i_{L1} \\ u_{C2} \\ i_{L4} \\ u_{C3} \\ i_{L3} \\ u_{C4} \end{bmatrix}
$$

$$
+ \begin{bmatrix} \frac{1}{R_{R1}} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & \frac{1}{R_{R10}} \end{bmatrix} \cdot \begin{bmatrix} u_{U1} \\ u_{U2} \end{bmatrix} + (\mathbf{A_1} - \mathbf{A_2}) \cdot \mathbf{X} \cdot \alpha \tag{50}
$$

$$
\begin{bmatrix} i_{Out} \\ u_{Out} \end{bmatrix} = \begin{bmatrix} \frac{1}{R_{R10}} \\ 1 \end{bmatrix} \cdot \begin{bmatrix} u_{C4} \end{bmatrix} + \begin{bmatrix} -\frac{1}{R_{R10}} \\ 0 \end{bmatrix} \cdot \begin{bmatrix} u_{U2} \end{bmatrix} \tag{51}
$$

5.3 Transfer Function

The power flow path of the battery management system has several transfer functions (Erickson; Maksimović, 2004; Horn; Dourdoumas, 2004), depending on what is defined as input and which output is considered. In the corresponding mathematical AC model (equation (50) and (51)) there are three variables that can be varied - u_{U1}, u_{U2} and α. In reality, U1 and U2 will not vary because these are high-capacity batteries with response times from several seconds to minutes, so we can set them to zero. For the closed-loop control, only the variation of the duty cycle α is of interest, and therefore, this will be the input of the control system. So, the general state-space representation with the two outputs i_{Out} and u_{Out} is shown in equation (52) and (53).

The outputs are the current i_{Out} and the voltage u_{Out} in the vector $\mathbf{y}(t)$. But to calculate this two transfer functions there is a small modification necessary. While for the calculation of i_{Out}/α the resistance of R10 has a value of $70.54\,\mathrm{m\Omega}$, R10 must be changed to $100\,\mathrm{k\Omega}$ to get a correct result for u_{Out}/α. The closed-loop control, that will control the voltage, takes over the control only at light load, when the output reaches the cell voltage or when the cell is disconnected. This high impedance respectively light load output state can be simulated by using a high resistance value for R10 (for example $100\,\mathrm{k\Omega}$) and leads to a new transfer function, since the strong damping of the LC resonant circuit (L3 and C4) no longer exists.

$$\mathbf{K} \cdot \frac{\mathrm{d}\mathbf{x}(t)}{\mathrm{d}t} = \mathbf{A} \cdot \mathbf{x}(t) + (\mathbf{A_1} - \mathbf{A_2}) \cdot \mathbf{X} \cdot \alpha(t) \tag{52}$$

$$\mathbf{y}(t) = \mathbf{C} \cdot \mathbf{x}(t) \tag{53}$$

$$\circ\!\!-\!\!\bullet$$

$$s \cdot \mathbf{K} \cdot \mathbf{x}(s) = \mathbf{A} \cdot \mathbf{x}(s) + (\mathbf{A_1} - \mathbf{A_2}) \cdot \mathbf{X} \cdot \alpha(s) \tag{54}$$

$$\mathbf{y}(s) = \mathbf{C} \cdot \mathbf{x}(s) \tag{55}$$

Equations (52) and (53) can be converted into the complex frequency domain (equations (54) and (55)) utilizing Laplace transformation (Horn; Dourdoumas, 2004). Rearranging of these equations provides a calculation rule (equation (56)) for the transfer function, where $\mathbf{g}(s) = \mathbf{y}(s)/\alpha(s)$. Due to the two different values for R10, the calculation of equation (56) must be done twice, and the corresponding result must be selected from the vector $\mathbf{g}(s)$.

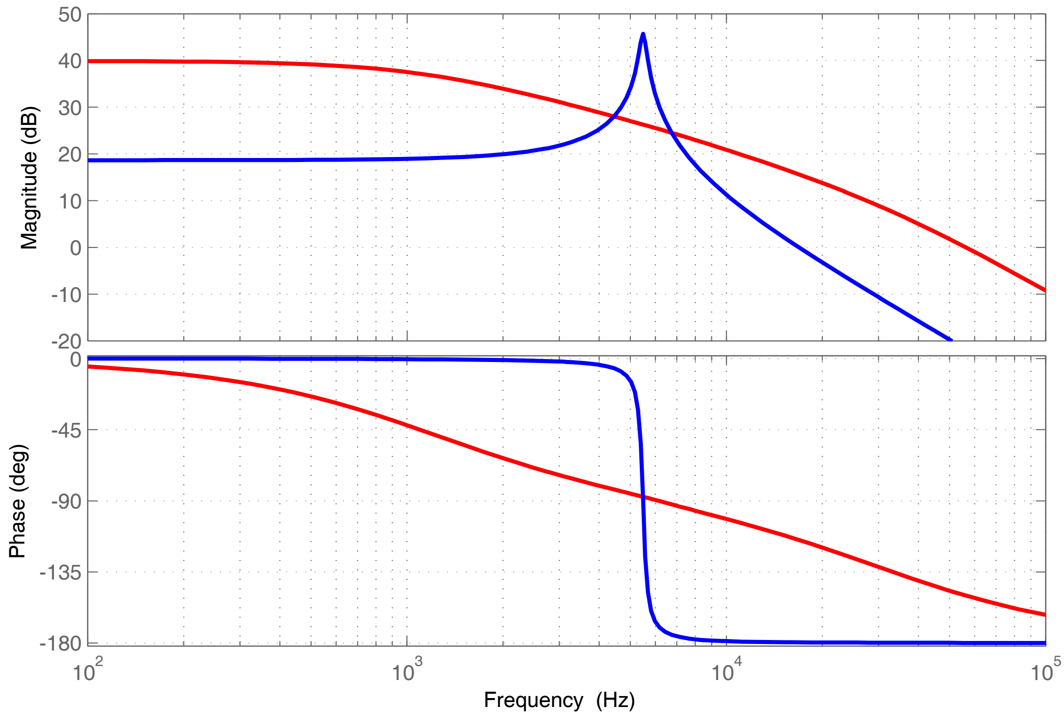
$$\mathbf{g}(s) = \mathbf{C} \cdot (s \cdot \mathbf{K} - \mathbf{A})^{-1} \cdot (\mathbf{A_1} - \mathbf{A_2}) \cdot \mathbf{X} \tag{56}$$

By the reason of the size of the matrix $(s \cdot \mathbf{K} - \mathbf{A})^{-1}$ only a computer-based calculation can solve the equation in a reasonable time. To further simplify the process, all known variables are replaced by their corresponding values from Table 4, Table 5 and Table 6. The calculation yields the two transfer functions $i_{Out,1}/\alpha$ with R_{R10} is $70.53\,\mathrm{m\Omega}$ and $u_{Out,1}/\alpha$, where R_{R10} is $100\,\mathrm{k\Omega}$ (equation (57) and (58)). Separated into magnitude and phase, this both curves can be displayed as a bode plot (Figure 35).[9] For this purpose the transfer function $i_{Out,1}/\alpha$ in Figure 35 is shown in red, while the color blue is used for $u_{Out,1}/\alpha$.

$$\frac{i_{Out,1}(s)}{\alpha(s)} = \frac{\begin{gathered}1.426\text{E}11 \cdot s^5 + 1.759\text{E}17 \cdot s^4 + 3.430\text{E}22 \cdot s^3 \\ + 9.615\text{E}27 \cdot s^2 + 3.519\text{E}32 \cdot s + 1.362\text{E}37\end{gathered}}{\begin{gathered}s^7 + 1.436\text{E}6 \cdot s^6 + 4.913\text{E}11 \cdot s^5 + 1.178\text{E}17 \cdot s^4 \\ + 1.644\text{E}22 \cdot s^3 + 6.872\text{E}26 \cdot s^2 + 2.293\text{E}31 \cdot s + 1.377\text{E}35\end{gathered}} \tag{57}$$

$$\frac{u_{Out,1}(s)}{\alpha(s)} = \frac{\begin{gathered}1.006\text{E}10 \cdot s^5 + 1.241\text{E}16 \cdot s4 + 2.419\text{E}21 \cdot s^3 \\ + 6.781\text{E}26 \cdot s^2 + 2.482\text{E}31 \cdot s + 9.602\text{E}35\end{gathered}}{\begin{gathered}s^7 + 1.235\text{E}6 \cdot s^6 + 2.427\text{E}11 \cdot s^5 + 6.911\text{E}16 \cdot s^4 \\ + 2.811\text{E}21 \cdot s^3 + 1.780\text{E}26 \cdot s^2 + 3.024\text{E}30 \cdot s + 1.121\text{E}35\end{gathered}} \tag{58}$$

Figure 35 – Pode-plot of the transfer functions $i_{Out,1}/\alpha$ (red) and $u_{Out,1}/\alpha$ (blue)



Source: by the author

While the push-pull converter and the input filter stages of the circuit can almost be neglected, the synchronous converter has the greatest influence on the curve shapes. The resonance frequency of around 5.4 kHz of the L3/C4 resonant circuit (Figure 34) is clearly recognizable, especially at low damping where $R_{R10} = 100\,\mathrm{k\Omega}$ (blue curve in Figure 35). This agrees with the calculation of the resonance frequency from equation (59).

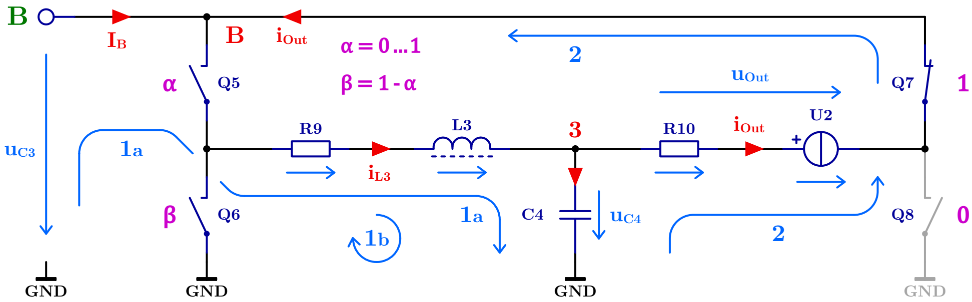
$$f_{res,Sync} = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{L3} \cdot C_{C4}}} = \frac{1}{2 \cdot \pi \cdot \sqrt{12.1\,\mathrm{\mu H} \cdot 70.40\,\mathrm{\mu F}}} = 5.453\,\mathrm{kHz} \tag{59}$$

[9] $s = j \cdot \omega + \sigma$, with $\sigma = 0 \rightarrow s = j \cdot \omega = j \cdot 2 \cdot \pi \cdot f$

5.3.1 Polarity Change

If the voltage polarity of u_{out} must be changed (depending on the selected battery cell and thus on the switching status of the multiplexer) and Q7 is switched on instead of Q8, the differential equations and thus the state-space representation also change. The reason for this are the varied nodes and meshes, as shown in Figure 36.

Figure 36 – Full-bridge stage replacement circuit - switch Q7 closed



Source: by the author

Compared to the formula (36), the new formula (60) of the mesh 2 has an additional u_{C3} term to close the loop. Furthermore, the term I_B changes because the current i_{Out} now also flows into node 3 (Figure 36). The basic equation for node 3 is therefore presented in formula (61).

$$
\begin{aligned}
&(2) \qquad 0 = -u_{C4} + u_{R10} + u_{U2} + u_{C3} &(60)\\
&(3) \qquad 0 = I_B - i_{L3} \cdot \alpha + i_{Out} &(61)
\end{aligned}
$$

Both formulas change the differential equations (33) and (39). The new equations are now

$$
C_{C3} \cdot \frac{\mathrm{d}u_{C3}}{\mathrm{d}t} = I_A \cdot \frac{1}{k} - u_{C3} \cdot \left(\frac{R_{R7} \cdot k^2 + R_{R8}}{R_{R7} \cdot R_{R8} \cdot k^2} + \frac{1}{R_{R10}} \right) - i_{L3} \cdot \alpha + \frac{u_{C4}}{R_{R10}} - \frac{u_{U2}}{R_{R10}}, \tag{62}
$$

$$
C_{C4} \cdot \frac{\mathrm{d}u_{C4}}{\mathrm{d}t} = u_{C3} \cdot \frac{1}{R_{R10}} + i_{L3} - u_{C4} \cdot \frac{1}{R_{R10}} + u_{U2} \cdot \frac{1}{R_{R10}}. \tag{63}
$$

In addition, the output equation of $\mathbf{y}(t)$ must also be adapted (equation (64) and (65)).

$$
i_{Out} = u_{C4} \cdot \frac{1}{R_{R10}} - u_{C3} \cdot \frac{1}{R_{R10}} - u_{U2} \cdot \frac{1}{R_{R10}} \tag{64}
$$

$$
u_{Out} = u_{C4} - u_{C3} \tag{65}
$$

With these modified equations, the state-space representation and the small-signal AC model can be regenerated and, as usual, new transfer functions for current and voltage can be calculated. This two transfer functions $i_{Out,2}/\alpha$ and $u_{Out,2}/\alpha$ describes the current and voltage variation in dependence of the duty cycle α and is only valid in the case that switch

Q7 is closed and Q8 is opened (negative voltage generation for u_{Out}). The corresponding polynomials are shown in equations (66) and (67).

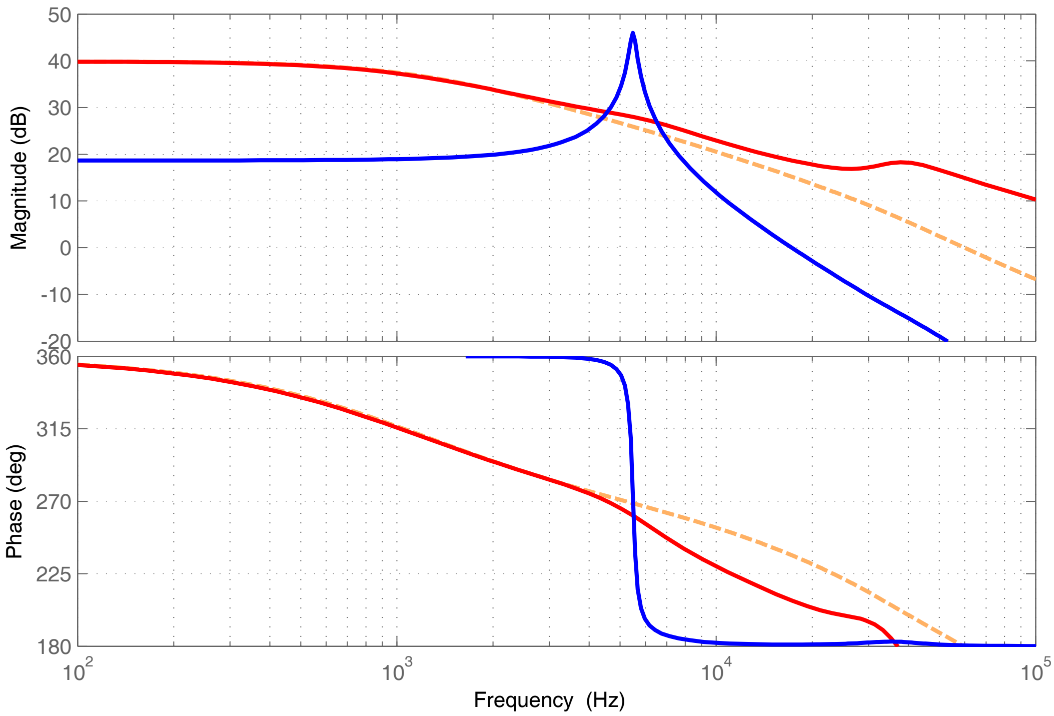
$$\frac{i_{Out,2}(s)}{\alpha(s)} = \frac{\begin{array}{r}-2.058\text{E}6 \cdot s^6 - 2.381\text{E}12 \cdot s^5 - 2.558\text{E}17 \cdot s^4 \\ - 5.269\text{E}22 \cdot s^3 + 6.810\text{E}27 \cdot s^2 + 3.583\text{E}32 \cdot s^1 + 1.261\text{E}37\end{array}}{\begin{array}{r}s^7 + 1.474\text{E}6 \cdot s^6 + 5.380\text{E}11 \cdot s^5 + 1.262\text{E}17 \cdot s^4 \\ + 1.811\text{E}22 \cdot s^3 + 7.532\text{E}26 \cdot s^2 + 2.294\text{E}31 \cdot s + 1.284\text{E}35\end{array}} \tag{66}$$

$$\frac{u_{Out,2}(s)}{\alpha(s)} = \frac{\begin{array}{r}-0.228 \cdot s^6 + 1.078\text{E}10 \cdot s5 + 1.330\text{E}16 \cdot s^4 \\ + 2.577\text{E}21 \cdot s^3 + 7.097\text{E}26 \cdot s^2 + 2.597\text{E}31 \cdot s + 9.602\text{E}35\end{array}}{\begin{array}{r}s^7 + 1.235\text{E}6 \cdot s^6 + 2.427\text{E}11 \cdot s^5 + 6.911\text{E}16 \cdot s^4 \\ + 2.811\text{E}21 \cdot s^3 + 1.780\text{E}26 \cdot s^2 + 3.024\text{E}30 \cdot s + 1.121\text{E}35\end{array}} \tag{67}$$

These two polynomial equations can also be separated into magnitude and phase and are presented in Figure 37 where the red color is used for $i_{Out,2}/\alpha$ and blue for $u_{Out,2}/\alpha$.

While the transfer function of the voltage is very similar to the curve in Figure 35, the current transfer function differs, especially at higher frequencies. The cause of this deviation are the different mesh and node from Figure 36 and, especially, the capacitor C3 with a capacitance C_{C3} of 376.2 µF. The capacitance is not large enough to connect the *VZK* potential sufficiently with the ground (*GND*) in terms of alternating current. Only through a significant increase in the capacity, the influence on the transfer function can be reduced and will be closer and closer to the bode plot from Figure 35. For example, the orange, dashed curve, which represents a capacity of 3762.0 µF, almost corresponds to the transfer function of $i_{Out,1}/\alpha$.

Figure 37 – Pode-plot of the transfer functions $i_{Out,2}/\alpha$ (red) and $u_{Out,2}/\alpha$ (blue)

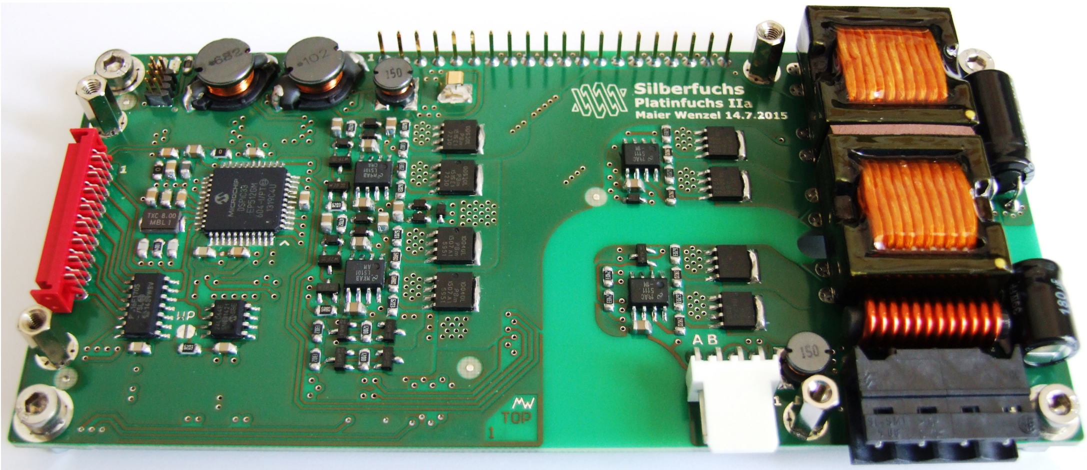


Source: by the author

6 DC/DC CONVERTER BOARD

The entire electronic with all sub-circuits, connectors and mechanical fastenings could be realized as a compact module with dimensions of 130 × 63 × 18 mm (without plugged connectors) and an approximate weight of 200 g. The module is called Silberfuchs battery management system and consists of two matched printed circuit boards (Platinfuchs IIa and Polarfuchs IIa). The power multiplexer board (Polarfuchs IIa) is plugged onto the DC/DC converter module as an add-on board. The DC/DC converter board is responsible for the energy conversion and is called Platinfuchs IIa (Figure 38).

Figure 38 – DC/DC converter board Platinfuchs IIa



Source: by the author

This chapter deals in detail with the power and control part implemented on the Platinfuchs IIa board (DC/DC converter) as well as with the measurements and the communication interfaces. The electronic is specially developed for low costs. For this purpose, inexpensive, readily available electronic components with standard housings (easy to assemble) are used. Only the transformer and the storage inductor are custom-made. These two inductors were designed to withstand high-temperatures (up to 125 °C) like the rest of the components. The high-temperature resistance of the prototype enables the battery management system to achieve a long lifespan at normal operating temperatures.[1]

Due to the standard housing, most components can easily be replaced by similar types from other manufacturers without changing the layout of the circuit board. In combination with the selectable switching frequency, this also enables the efficiency of the balancer electronic to be optimized for the desired operating point. In addition, parts of the circuit can be redesigned according to requirements to adapt the function, performance and/or costs of the electronic.

[1] The continuous operating temperature of the connectors and LEDs are 100 °C and 85 °C.

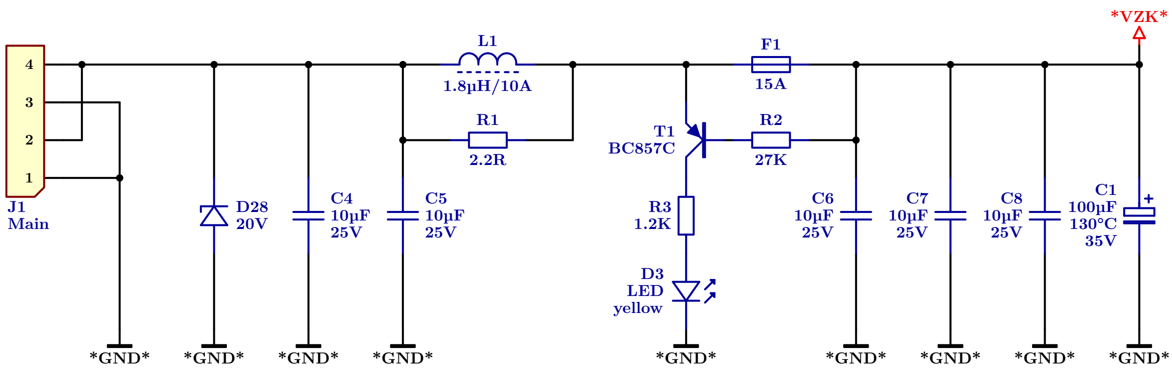
6.1 Input Filter

The +12 V main power supply not only supplies the Silberfuchs battery management unit, but typically also additional electronic units (e.g. in a vehicle electrical system). This electronic must be protected from radiated interferences caused by the fast switching processes of the power converter stages used. Therefore, a power filter stage for the Platinfuchs IIa board is necessary.

6.1.1 PI Filter and Safety Fuse

The push-pull power conversion stage and the synchronous converter used will generate strong switching noise, especially at the primary side. To reduce noise and electromagnetic radiation on the main power cable, an input filter is integrated on the printed circuit board. Figure 39 shows this input stage. The input capacitors C4 and C5, inductor L1 and the output capacitors C6, C7 and C8 forms an PI filter with a cut-off frequency of approximately 26 kHz.[2]

Figure 39 – Input stage with PI filter and fuse indicator



Source: by the author

To keep losses as low as possible, a power inductor with only 3 mΩ resistance for L1 is used. In parallel, the damping resistor R1 suppresses self-oscillating of the filter stage. Transient voltage spikes on the cable will be absorbed by the Zener diode D28, and slow input voltage changes are smoothed out by the high temperature 100 µF electrolytic capacitor C1. C1, with C6, C7 and C8, also works as an energy reservoir for the following push-pull-converter (DC-link capacitor of the primary side).

To prevent a cable fire, a 15 A safety fuse is also implemented. The fuse F1 does not protect the semiconductors in the power circuit, but if a MOSFET is driven incorrectly or damaged, the fuse - as the weakest link - separates the electronic from the main source and prevents a catastrophic fire of the cable or in the electronic. The small circuit of T1, R2, R3 and D3 visualizes the condition of the fuse. If LED D3 (light-emitting diode D3) lights up, the fuse has been triggered and must be replaced.

[2] To suppress frequencies greater than 5.0 MHz a ferrite choke on the cable is helpfully.

6.2 Push-Pull Converter System

The 12 V supply and the accumulator cell to be balanced have different potentials from one another. Depending on the structure of the battery (numerous cells connected in series), the battery stack that the balancer monitors and the selected cell can have a potential difference up to ±800 V. Therefore, an electrical isolation for energy and data must be integrated in the system.

6.2.1 Bidirectional Push-Pull Converter

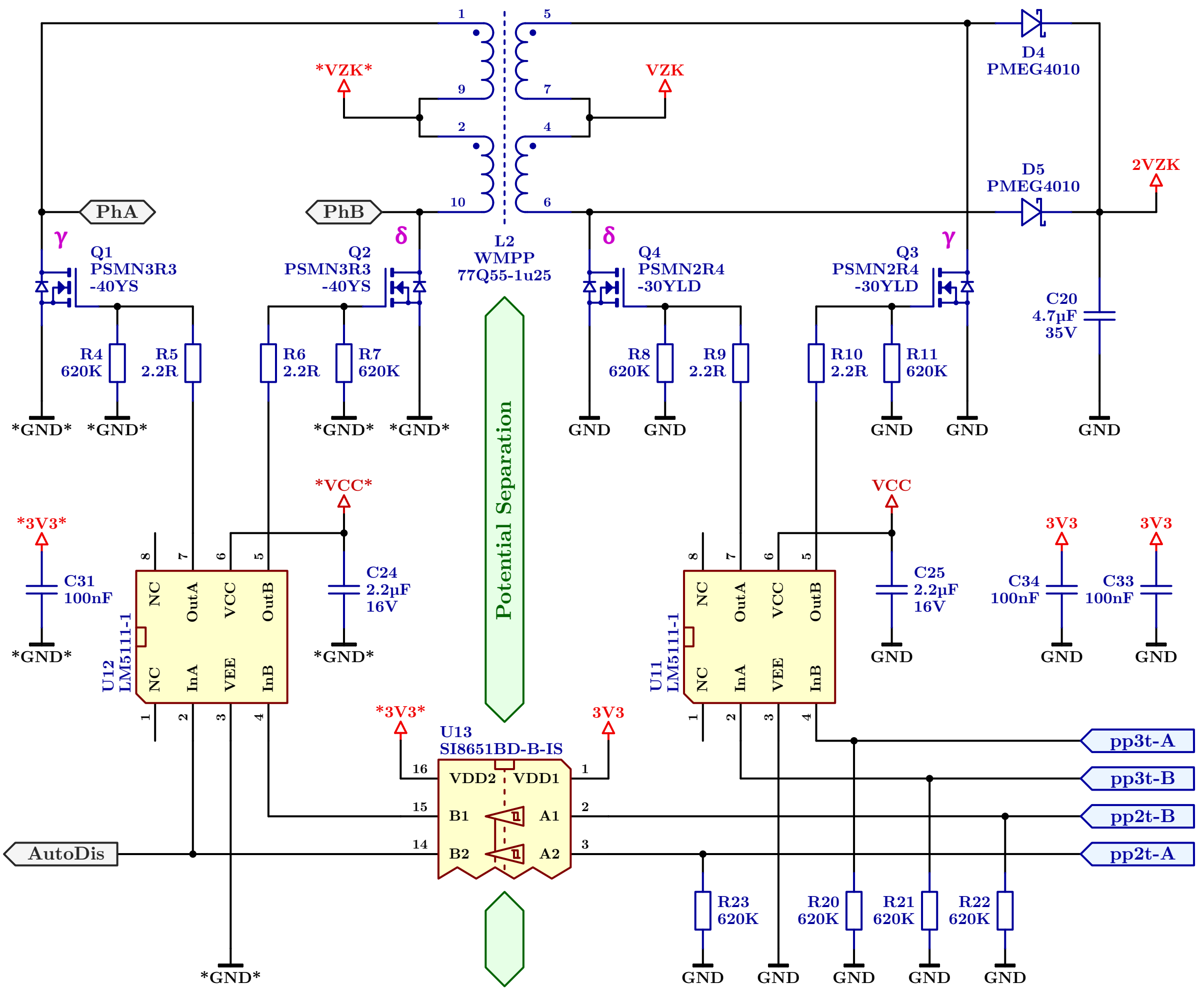
To achieve an electrical potential separation between the +12 V main supply and the battery stack, an energy conversion is essential. The push-pull circuit in Figure 40 converts the DC-link potential **VZK** to a square-wave voltage and, through the transformer L2, to a varying magnetic flux. This magnetic flux induces an alternating voltage on the secondary side of the transformer and is then reconverted by a synchronous rectifier to the new DC-link potential *VZK*. Due to the use of an optimized transformer and the synchronous rectification, the energy transfer works with high efficiency (>95 %).

The primary and secondary side of the converter are built up symmetrically. So, an energy transfer in both directions is possible. To transmit energy to the secondary side, the MOSFETs Q1/Q2 chops U_{*VZK*} and Q3/Q4 rectifies the generated AC voltage. If energy is transmitted to the primary side, Q3/Q4 chops U_{VZK} and Q1/Q2 works like a synchronous rectifier. In normal operation, when the MOSFETs Q1/Q2 and Q3/Q4 are synchronized and controlled by a fix duty cycle of $\gamma = 0.5$ and $\delta = 0.5$, the circuit works like a DC transformer with a transfer ratio of 0.714 29 (WMPP77Q55-1u25 transformer: $n_{sec,L2}/n_{pri,L2} = 5/7$). Because of the fix transfer factor of the converter, a variation of the **VZK** voltage on the primary side will also vary the *VZK* voltage on the secondary side and vice versa. Therefore, the transfer ratio is chosen so that a minimum input voltage will generate sufficient output voltage to supply the subsequent electronic. At a minimum primary input voltage of 7.50 V the secondary side will produce 5.36 V, which is more than enough to charge a selected accumulator cell to the maximum permissible final charge voltage. The maximal allowed input voltage of the converter is 16.50 V (secondary side: 11.79 V). So, a wide input voltage range is supported by the Platinfuchs IIa board and an ordinary 12 V battery can be used for the main power supply.[3]

Every power MOSFET in Figure 40 needs a gate driver to charge and discharge the gate capacitors in short time. The two drivers on the primary side and the two drivers on the secondary side are integrated in the semiconductor chips U11 and U12 and needs two different power supplies **VCC** and *VCC*. The switch-on and -off times of the power semiconductor depends on the gate charge of the power MOSFETs used, the gate resistors

[3] The electronic is optimized for a nominal U_{*VZK*} of 12.00 V respectively 8.57 V for U_{VZK} and delivers there the highest efficiency.

Figure 40 – Bidirectional push-pull converter with synchronous rectification



Source: by the author

(R5, R6, R9 and R10) and the voltage of **VCC** respectively *VCC*. U_{*VCC*} and U_{VCC} are adjustable to be optimized for the used power semiconductors (please refer subsection 6.5.1 and subsection 6.5.4).

To have full control over the push-pull converter, four control signals are required. Since the control system is located on the secondary side, the two signals *pp2t-A* and *pp2t-B* must be transferred to the primary side over the electrical isolation. For this, two channels of the capacitive five-channel digital isolator SI8051BD-B-IS (U13), which bridges the isolation barrier, are used. The other two signals, *pp3t-A* and *pp3t-B*, are connected directly to the gate driver U11 on the secondary side. The four control signals are pulse-width modulation (PWM) signals, which the digital control system respectively the microcontroller has to deliver. Each signal pair *pp2t-A*/*pp2t-B* and *pp3t-A*/*pp3t-B* get a PWM signal with a fixed duty cycle of 50 % ($\gamma = 0.5$ and $\delta = 0.5$). Only a small dead-time of 125 ns between the two phase signals are implemented to prevent the MOSFETs from a short circuit during the switching process.

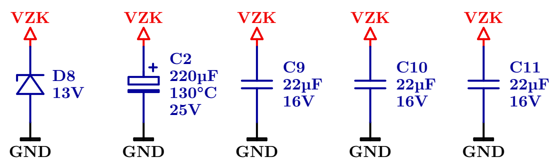
The switching frequency f_{sw} of a full PWM cycle is set by software and can vary within a wide range. However, to achieve best results, the frequency must be matched to the transformer L2. The transformer WMPP77Q55-1u25 is specially designed for a switching frequency of 120 kHz which leads to a switch-on time per phase of 4.167 µs at a duty cycle of 50 %. The flexible choose of the switching frequency f_{sw} and the pulse width makes it possible to reduce switching losses when the electronic unit is in standby or in monitoring mode. For this purpose, the duty cycle can be changed to 10 % ($\gamma = 0.1$ and $\delta = 0.1$) and the switching frequency is reduced to 24 kHz. This values also indicates a switch-on time of 4.167 µs where the necessary energy is being transferred to the secondary side. But now, between the switch-on pulses, there are 16.667 µs without energy transfer. To further reduce the losses, the synchronous rectifier can be switched off. To achieve this, only the control signals of *pp3t-A* and *pp3t-B* must be disabled. In this case, the build in diode of the MOSFETs Q3 and Q4 take over the rectification function.

Normally, the MOSFETs Q1/Q2 on the primary side and the MOSFETs Q3/Q4 on the secondary side works synchronous and no phase delay is required. Due to the stray inductance ($L_{\sigma,pri,L2} = 241\,\text{nH}$) of the transformer L2 and the propagation delay of the digital isolator U13 a small phase shift between the pp2t and pp3t signal pairs can be added by the microcontroller. To optimize the switching process, this phase shift can be actively adjusted by the controller.[4]

6.2.2 DC-Link Capacitors

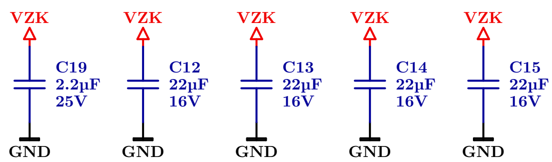
For the correct function of the push-pull converter circuit from Figure 40 a primary and a secondary DC-link capacitor bank are necessary. These capacitors temporarily stores energy and stabilize the **VZK** and *VZK* voltages. On the primary side C6, C7, C8 and the electrolytic capacitor C1 (Figure 39) are not only for the input filter. They also couple the filter stage with the push-pull converter energetically. On the secondary side, the push-pull and the synchronous converter are coupled in terms of energy by the capacitors in Figure 41 and Figure 42.

Figure 41 – Push-pull DC-link capacitors



Source: by the author

Figure 42 – Full-bridge DC-link capacitors



Source: by the author

To achieve low inductance in the DC-links, multiple high capacity ceramic capacitors are connected in parallel and mounted as close as possible to the power stages. Due to the different positioning of the push-pull and the synchronous converter on the PCB, the

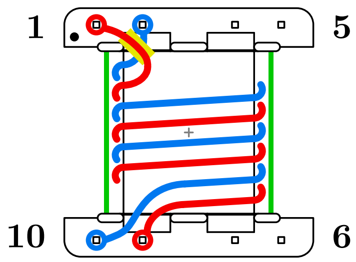
[4] This function is currently not implemented in software.

secondary capacity bank was split up. The capacitors from Figure 41 are mounted close to the secondary side of the push-pull converter and the capacitors of Figure 42 are positioned near the synchronous converter. The two high temperature electrolytic capacitors C1 and C2 with their large capacitance are built in to absorb and emit larger power peaks to damp load jumps on the input and output side.

6.2.3 Transformer Construction

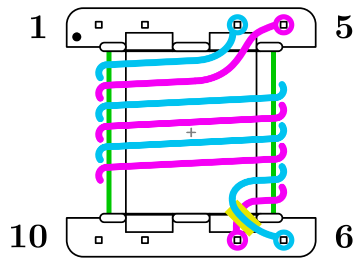
The transformer L2 is the main part of the push-pull converter and must design carefully to achieve a good potential separation and a high efficiency. Because of the compact design and small footprint, an EFD20 ferrite core with N97 material was chosen. At a switching frequency of 100 kHz this EFD20 ferrite can deliver up to 120 W to the secondary side. That is more than twice as much power as the maximum intended for balancing. To reduce the core losses at lower temperatures in the range of 20 °C to 80 °C the N97 material can be replaced by N95, 3C95 or similar materials. The bobbin, where the cooper windings will be mounted, was modified to achieve higher clearance and creepage distances. Therefore, the pins 3 and 8 were removed (Figure 43 and Figure 44) so a distance of at least 5.00 mm between primary and secondary side is possible.

Figure 43 – Winding scheme, primary side



Source: by the author

Figure 44 – Winding scheme, secondary side



Source: by the author

To use the transformer for a push-pull converter, two windings with a center tap are needfully. These windings are split into two separate parts so that the transformer will have in total four windings. The center taps are realized by connecting the pins 2 and 9 as well as 4 and 7 direct on the printed circuit board (see circuit board layout). This two points corresponds to the **VZK** and *VZK* potentials. Because of the skin and proximity effects at high frequencies, the cooper windings must be designed as a high-frequency stranded wire. A silk-braided high-frequency litz wire with 0.1 mm single wires has proven to be ideal because it is compact, easy to mount and can be soaked with protective varnish.[5] The litz wire used withstands temperatures of up to 155 °C and is manufactured by Rudolf Pack GmbH & Co. KG (Rupalit® Classic Plus). The correct winding scheme for the primary and secondary coils is shown in Figure 43 and Figure 44 (bottom view).

[5] The litz wire used consists of many insulated thin wires with a diameter of 0.1 mm, which are twisted together.

As can be seen in the figures, the coils on the secondary side are wound directly over the primary side coils to enable low stray inductance. Between the primary and secondary side two layers of aramid foil (NOMEX® 410 from DuPont de Nemours, Inc.), each 80 µm thick, are used to improve the isolation (green bar in Figure 43 and Figure 44). This material has a low-loss factor and a dielectric constant ϵ_r of 1.6. In order to improve the insulation properties, the aramid paper was also impregnated with an AC41 insulation varnish ($\epsilon_r = 2.0$). The low dielectric constants of the insulating paper and varnish reduces the capacity between the primary and secondary side to a minimum. The AC41 varnish (Von Roll Holding AG) was also used to fix, isolate and protect the ferrite core. The fully soaked and dried transformer was tested with a DC voltage of 2400 V between the primary and secondary side for one minute ($I_{leak,L2} < 0.1\,\mu A$). According to the information of the company RECOM Power GmbH, the isolation of the transformer is sufficient for a continuous operating voltage of 1100 V.

The peak magnetic flux density $B_{max,L2}$ in the transformer can be calculated by equation (68) or (69), where the cross-section of the ferrite core $A_{e,L2}$ is 31 mm^2. Since the iron losses of the ferrite increase sharply with higher flux density, the core should only be operated with a third or half of the maximum permitted flux density (N97 material: $B_{sat} = 400\,mT$). At a typical voltage of 12 V for U_{*VZK*} and 7 turns for the primary coil, the magnetic flux density $B_{max,L2}$ will be 115.21 mT. Because the **VZK** voltage can vary in the range of 7.50 V to 16.50 V $B_{max,L2}$ will also vary between 72.00 mT and 158.41 mT (equation (68)).

$$B_{max,L2} = \frac{U_{*VZK*}}{4 \cdot n_{pri,L2} \cdot f_{sw} \cdot A_{e,L2}} = \frac{12.00\,\mathrm{V}}{4 \cdot 7 \cdot 120\,\mathrm{kHz} \cdot 31\,\mathrm{mm}^2} = 115.21\,\mathrm{mT} \tag{68}$$

$$B_{max,L2} = \frac{U_{VZK}}{4 \cdot n_{sec,L2} \cdot f_{sw} \cdot A_{e,L2}} = \frac{8.57\,\mathrm{V}}{4 \cdot 5 \cdot 120\,\mathrm{kHz} \cdot 31\,\mathrm{mm}^2} = 115.19\,\mathrm{mT} \tag{69}$$

With 5 turns on the secondary side the transformer, designated as WMPP77Q55-1u25, has a transfer radio of 0.714 29 ($n_{sec,L2}/n_{pri,L2} = 5/7$). To keep the resistance loss low, the entire winding space was used for the copper winding. The most important characteristics of the coil system of the transformer WMPP77Q55-1u25 are shown in Table 7 (including measured copper resistance).

Table 7 – Winding characteristics of transformer WMPP77Q55-1u25

	phase	label	pins	turns	litz wire	cross-section	resistance
Pri.:	A	$n_{pri,L2a}$	1-9	7	$45 \cdot 0.1$	0.35 mm^2	12.92 mΩ
	B	$n_{pri,L2b}$	2-10	7	$45 \cdot 0.1$	0.35 mm^2	12.78 mΩ
Sec.:	A	$n_{sec,L2a}$	5-7	5	$90 \cdot 0.1$	0.71 mm^2	5.96 mΩ
	B	$n_{sec,L2b}$	4-6	5	$90 \cdot 0.1$	0.71 mm^2	5.81 mΩ

Source: by the author

Should it be necessary to further reduce the copper losses, the winding system can be modified. As can be seen in Table 8 the transformer WMPP66Q55-1u25 uses fewer turns and a larger cross-section of the litz wire. Thereby, at a switching frequency f_{sw} of 120 kHz, the peak magnetic flux density will reach 134.41 mT (84.00 mT at 7.50 V respectively 184.81 mT at 16.50 V). This can be compensated by increasing f_{sw} but also will give higher switching losses at the power MOSFETs.

Table 8 – Winding characteristics of transformer WMPP66Q44-1u25

	phase	label	pins	turns	litz wire	cross-section	resistance
Pri.:	A	$n_{pri,L2a}$	1-9	6	$60 \cdot 0.1$	0.47 mm^2	8.35 mΩ
	B	$n_{pri,L2b}$	2-10	6	$60 \cdot 0.1$	0.47 mm^2	8.20 mΩ
Sec.:	A	$n_{sec,L2a}$	5-7	4	$120 \cdot 0.1$	0.94 mm^2	3.61 mΩ
	B	$n_{sec,L2b}$	4-6	4	$120 \cdot 0.1$	0.94 mm^2	3.52 mΩ

Source: by the author

The main inductance on the primary side of the transformer WMPP77Q55-1u25 can be calculated by $L_{M,pri,L2} = n^2_{pri,L2} \cdot A_{L,L2}$ and is 61.25 µH ($A_{L,L2} = 1.25$ µH). The primary side leakage inductance $L_{\sigma,pri,L2}$ is 241 nH (measured directly in the circuit). Transformer WMPP66Q44-1.25 has a main inductance of around 45.00 µH. The stray inductance was not measured and is unknown.

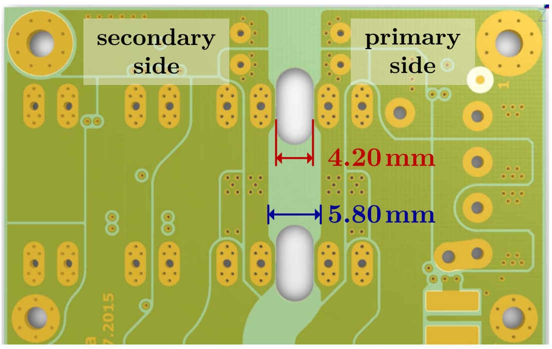
6.2.4 Potential Separation

The electrical isolation barrier between the primary and secondary side is bridged by only two components. The push-pull transformer L2 is used to transfer energy, while the digital isolator U13 is responsible for the data. The SI8051BD-B-IS chip allows a maximum working insulation voltage of 1200 V and the transformer WMPP66Q44-1u25 was tested with 2400 V for one minute (1100 V continuous insulation operating voltage). To achieve these insulation values, both components are completely encapsulated in plastic so that neither dirt nor humidity can affect the potential separation.

The PCB of the DC/DC converter was designed so that a minimum creepage distance of 5.80 mm is maintained. However, since the pin spacing between the primary and secondary side of the transformer is too small for this, a 4.20 mm slot was milled into the circuit board to increase insulation capability (Figure 45). This 4.20 mm clearance distance is also the minimum distance in air between the EIA-485 connector J2 and the cell stack connector (plug-in connector on the multiplexer board).

According to the international norms IEC 60071 and IEC 60664, a clearance distance of 4.00 mm (overvoltage category II respectively required impulse voltage of 5000 V plus inhomogeneous electric field) and a creepage of 5.60 mm (insulation material II plus pollution degree 2) is sufficient for a working insulation voltage up to ±800 V. Since the

Figure 45 – Clearance and creepage distances



Source: by the author

battery system typically has a positive (U_{Bat+}) as well as a negative (U_{Bat-}) voltage relating to the earth potential, the balancer can be used for a total battery voltage up to 1600 V. However, if the positive or negative pole of the battery is connected to the same potential as the primary side of the Silberfuchs balancer, only 800 V are permitted.

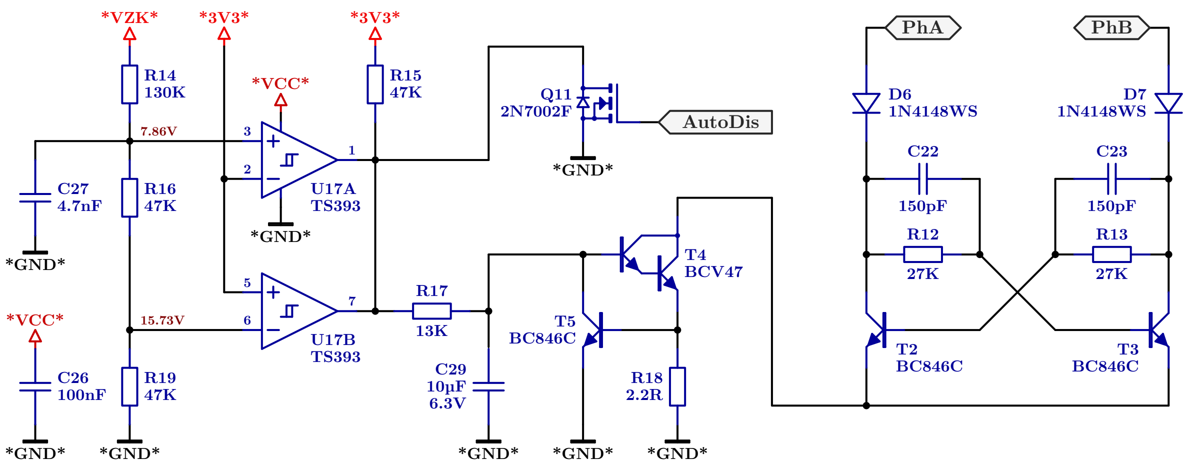
6.2.5 Autostart Circuit

At the first moment, when the battery management system is supplied with energy, the secondary side of the DC/DC converter is without power. Unfortunately, the digital control system on the secondary side requires energy to start-up and generates the signals to control the push-pull converter. A common solution will be to use an independent low-power supply with a small transformer to supply the digital control system. But this will be an expensive solution because an extra isolation transformer must design special to withstand the high voltage of ±800 V between the primary and secondary side. It is therefore an advantage to use the transformer L2 of the push-pull converter to power the secondary side. In order to be able to supply the secondary side with energy during the start-up process, a special automatic start-up circuit was developed. The Autostart circuit in Figure 46 works only a few seconds until the digital control system is ready to take over the control of the push-pull converter. Therefore, only simple and cheap components are used for this circuit.

The left side of the circuit is a window comparator that deactivates the start-up process if the input voltage is outside the permissible range (<7.86 V or >15.73 V). After the start-up process, the digital control system (microcontroller system) is responsible for over- and under-voltage detection. If this over-/under-voltage protection is not necessary the components R14, R16, R19 C26, C27 and U17 does not have to be equipped on the PCB.

The current sink circuit in the middle of the schematic diagram, build up by the components R15, R17, R18 C29, T4 and T5, is normally always active. Only when MOSFET Q11 (or one of the comparator outputs) discharge capacitor C29, the circuit

Figure 46 – Autostart self oscillating circuit



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will be disabled. The *AutoDis* signal do turn on Q11 is generated by the PWM signal *pp2t-A* (Figure 40) and deactivates the Autostart circuit when the microcontroller takes over the control of the push-pull converter. Because the *AutoDis* signal consists of pulses, a switch-on delay is needfully. This is realized by an RC low-pass filter (R15, R17 and C29).

The right side of Figure 46 is a part of a self-oscillating push-pull oscillator (modified royer converter). With the current sink circuit and the power transformer L2, an alternating current with a frequency of around 250 kHz is generated. The actual resonance frequency depends on the main inductance $L_{M,pri,L2}$ and the drain-source capacity of the power MOSFETs Q1 to Q4 and can vary in a large range. By the high switching frequency and the linear regulation (current sink circuit) the energy transfer is not very efficient, but this circuit will be only active at the start-up time. After start-up, when the Autostart circuit is disabled, the diodes D6 and D7 decouples the circuit from the power stage. Otherwise, the push-pull converter will supply and damage the self-oscillating circuit.

The Autostart circuit supplies only a little amount of energy to the secondary side - just enough for start-up the digital control system. Therefore, the converter output must be switched off so that the energy is not consumed by a possible load at the output. Because the digital control system has full control over the power stages, unnecessary consumers can be deactivated during the start-up process. Thus, the Autostart circuit, in combination with the control of the microcontroller, is a simple and cost-effective solution to start the entire electronic unit.

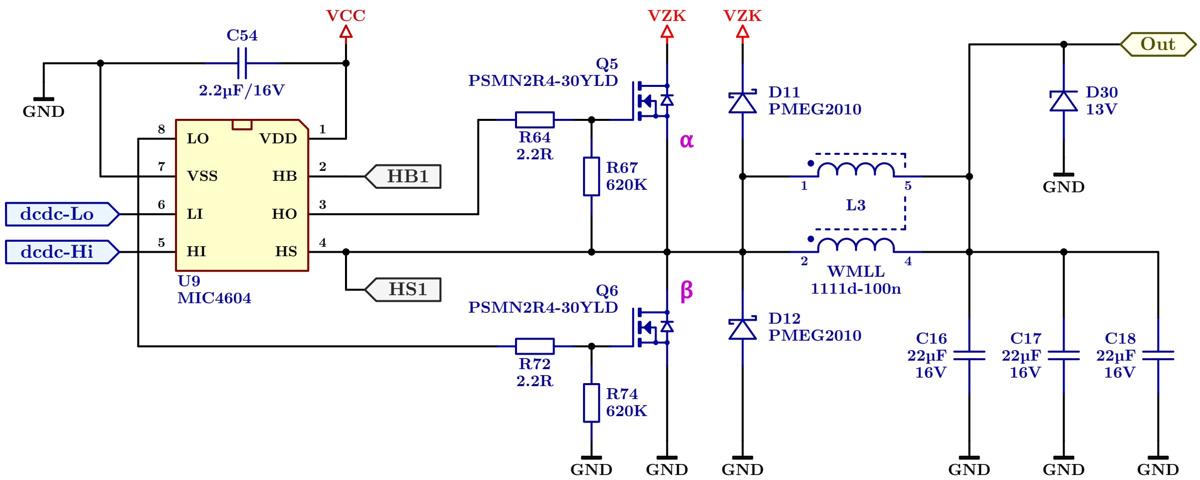
6.3 Full-Bridge Converter System

The *VZK* potential generated by the push-pull converter differs considerably from the desired cell voltage. If this voltage were switched directly to the accumulator cell, uncontrolled compensation currents will flow and inevitably destroy the electronic. Because of this, an extra energy converter stage is necessary and implemented at the Platinfuchs IIa board. This power stage is structured similarly to a full-bridge (H-bridge) and must perform several tasks. First, this power stage must transfer energy in both directions to charge and discharge the selected cell. Second, a current limitation to control the charge and discharge current to/from the accumulator cell is necessary (closed-loop control for the power stage). Third, the voltage from the *VZK* DC-link must be adjusted to the voltage of the cell. Fourth, depending on the selected cell and the corresponding switch status of the multiplexer (Polarfuchs IIa attachment board) the cell voltage can be positive or negative. Hence, the electronic must create a corresponding voltage polarity.

6.3.1 Synchronous Converter

Since the voltage from the *VZK* DC-link is always greater than the voltage of the cell, a synchronous converter is used to adapt the two voltages to one another. The circuit in Figure 47 enables bidirectional energy transfer with good efficiency. When energy is transferred to the accumulator cell (*VZK* to *Out*), the circuit runs like a buck (step-down) converter, where the MOSFET Q6 replaces the typical flyback diode and works as a synchronous rectifier. In boost mode (step-up) the energy will flow from the cell back to the *VZK* DC-link (*Out* to *VZK*). In this case, the MOSFET Q5 is the flyback diode. The small voltage drop of the synchronous rectification (MOSFET) compared to diodes allows high efficiency in buck and boost mode ($> 95\,\%$).

Figure 47 – Synchronous converter



Source: by the author

The synchronous converter from Figure 47 is built up by discrete components. Only for the high-low side MOSFET driver (U9) an integrated circuit is used. So, every part, especially the MOSFETs and power inductor L3, can be chosen and optimized to achieve the lowest costs or highest efficiency. The coil WMLL1111d-100n (L3) is custom-made and uses, equal like the transformer L2, an EFD20 ferrite core respectively bobbin. Both independent winding systems of the inductor are interconnected as shown in Figure 47 to achieve higher current carrying capacity and lower losses. The Schottky diodes D11 and D12 parallel to the MOSFETs allow a quick commutation of the inductor current and should reduce oscillation at the switching node. Since the output capacitors C16, C17 and C18 are not sufficient to absorb the stored energy of the inductance L3 if a load shedding, the Zener diode D30 was added. This absorbs the energy when the load is switched off by the multiplexer.

The circuit is controlled by the two PWM signals *dcdc-HI* and *dcdc-Lo* with a switching frequency f_{sw} of 120 kHz. The duty cycles α and β can be varied between 0 % and 100 % respectively 0 and 1 where the signals *dcdc-Hi* and *dcdc-Lo* are alternately high ($\beta = 1 - \alpha$). This will generate a voltage between zero and U_{VZK} at the connection *Out*. To prevent the MOSFETs from a short circuit during the switching phase, a small dead-time between the two control signals is necessary. The correct 120 kHz PWM signals with corresponding duty cycles and a dead-time of 275 ns are generated directly by the digital control system (microcontroller).

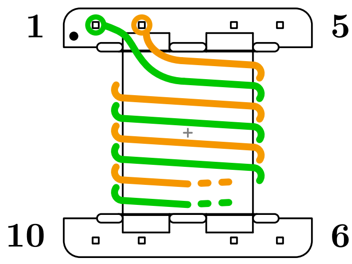
Because the synchronous converter does not have a discontinuous current mode, the current can reverse the direction at light load respectively low currents. Therefore, the power losses will increase slightly compared to buck-/boost topologies with diodes. In contrast, the continuous current mode (CCM) of the converter guarantees a linear relationship between the duty cycle and the voltage on *Out* at every time, which simplifies the closed-loop control notably.[6] To control the current to charge and discharge the cell and, at light load, the voltage, a closed-loop control is necessary. This control unit is implemented by an algorithm in the microcontroller (digital control) and must work in real time in four quadrants (charge/discharge current and positive/negative cell voltage).

6.3.2 Inductor Construction

The power inductor L3, like the transformer L2, uses an EFD20 ferrite core with an associated bobbin. The bobbin used has also been modified by removing pins 3 and 8. As can be seen in Figure 48 and Figure 49 (bottom view) the winding is split into two independent coils with the same number of turns. By mounting L3 on the PCB, the pins 1 and 2 as well as 4 and 5 will be interconnected and both coils works in parallel. By dividing and then connecting the coils in parallel, the winding space of the EFD20 core system can be optimally used, and the connection resistance reduced by half (two pins parallel). For the electronic circuit, there seems to be only one single coil with a correspondingly large copper cross-section.

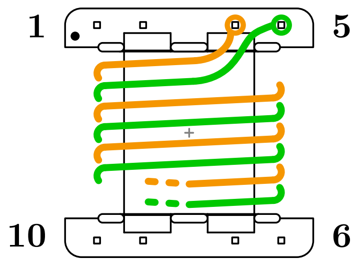
[6] If necessary the microcontroller can emulate a buck respectively boost converter with diodes by disabling the PWM control signal for the corresponding MOSFET. Therefore, the build in diode of the MOSFET will operate as the flyback diode.

Figure 48 – Winding scheme, bottom layer



Source: by the author

Figure 49 – Winding scheme, top layer



Source: by the author

Compared to a transformer, the current flow in a storage choke changes only slightly. If the inductance is correctly designed, a ripple current $I_{\Delta,L3}$ (approximately 20 % to 30 % of the maximum rated current) is added to the direct current. Therefore, a high-frequency stranded wire is not necessary, since the skin and proximity effects occurs only slightly. Nevertheless, a silk-braided litz wire with 0.1 mm single wires, like for L2, is used to wind the coils on the bobbin. Due to the simple production (winding the coil and soldering on the connection pins) the high-frequency stranded wire was preferred to a solid wire with the appropriate cross-section. The coils are spread over two layers, whereby the PWM signal, generated by the power MOSFETs Q5 and Q6, acts on the lower winding (Figure 48) and is shielded by the upper winding (Figure 49). This helps to reduce noise and electromagnetic radiation to the environment. In order to increase the mechanical stability, the finished power inductor with the coil system and the ferrite core was dipped in AC41 protective varnish.

The ripple current $I_{\Delta,L3}$ will also produce a variable magnetic flux in the ferrite core. There, however, this magnetic flux is only 20 % to 30 % of the constant flux, that means that the hysteresis curve is small and a cheaper ferrite core material can be used. TDK Electronics Co, Ltd produces EFD20 cores with N87 material with integrated air gap. This air gap $l_{air,L3}$ is necessary to store the magnetic energy. So, a N87 - EFD20 core with an air gap $l_{air,L3}$ of 0.49 mm was chosen for the inductor design (3C95 ferrite material from Ferroxcube International Holding B.V. will also work).

The maximal allowable current $I_{max,L3}$ in the inductor can be calculated by equation (70), where $B_{max,L3}$ must be less than or equal to B_{sat} otherwise the core will be saturated (for N87 material: $B_{max,L3} = B_{sat} = 370mT$). From the peak current, the half ripple current $I_{\Delta,L3}$ must still be subtracted to get $I_{DC,L3}$. $I_{DC,L3}$ is the maximal operating direct current of the inductor and also the maximal current with which the accumulator cell can be balanced. The ripple current $I_{\Delta,L3}$ can be calculated by equation (71). For worst-case condition, U_{VZK} in the equation (71) is the maximal voltage that can occur on the secondary side ($U_{VZK} = 11.79\,\text{V}$) and U_{Out} is half of U_{VZK}.

$$I_{max,L3} = \frac{B_{max,L3} \cdot l_{air,L3}}{\mu_0 \cdot n_{L3}} = \frac{370\,\mathrm{mT} \cdot 0.49\,\mathrm{mm}}{4 \cdot \pi \cdot 10^{-7}\,\mathrm{N/A^2} \cdot 11} = 13.12\,\mathrm{A} \tag{70}$$

$$I_{\Delta,L3} = \frac{U_{Out}}{L_{L3} \cdot f_{sw}} \cdot \left(1 - \frac{U_{Out}}{U_{VZK}}\right) = \frac{5.90\,\mathrm{V}}{12.10\,\mu\mathrm{H} \cdot 120\,\mathrm{kHz}} \cdot \left(1 - \frac{5.90\,\mathrm{V}}{11.80\,\mathrm{V}}\right) = 2.03\,\mathrm{A} \tag{71}$$

The inductance can be easily calculated by $L_{L3} = n_{L3}^2 \cdot A_{L,L3}$, where the $A_{L,L3}$ value for the ferrite core with an air gap of 0.49 mm is given in the data sheet ($A_{L,L3} = 100\,\mathrm{nH}$). Table 9 presents four possible numbers of turns, their calculated current limits, the litz wire structure and the total resistance. The power inductor WMLL1111d-100n used uses 11 turns and allows a direct current up to 12.11 A (Table 9). This inductor can be easily substituted by another to reduce the resistance and thus the losses.

Table 9 – Possible turns and associated values for the storage choke

n	L_{L3}	$I_{max,L3}$	$I_{\Delta,L3}$	$I_{DC,L3}$	litz wire	cross-section	resistance
8	6.40 µH	18.03 A	3.84 A	16.11 A	$2 \cdot 120 \cdot 0.1$	1.89 mm^2	3.70 mΩ
9	8.10 µH	16.03 A	3.03 A	14.52 A	$2 \cdot 90 \cdot 0.1$	1.41 mm^2	4.84 mΩ
10	10.00 µH	14.43 A	2.46 A	13.20 A	$2 \cdot 90 \cdot 0.1$	1.41 mm^2	5.26 mΩ
11	12.10 µH	13.12 A	2.03 A	12.11 A	$2 \cdot 75 \cdot 0.1$	1.18 mm^2	7.13 mΩ

Source: by the author

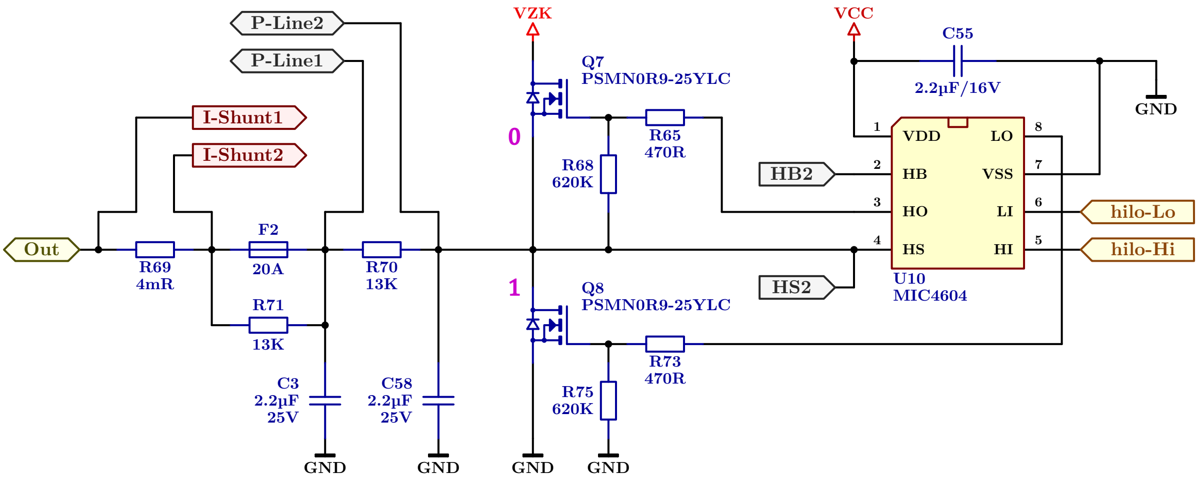
6.3.3 High-Low Selection Circuit

The high-low selection circuit in Figure 50 is a half-bridge made up of two discrete power MOSFETs Q7/Q8 and the associated MOSFET driver U10. Depending on the selected accumulator cell and the corresponding switch status of the Polarfuchs IIa multiplexer board, the low side switch Q8 (positive cell voltage) or the high-side switch Q7 (negative cell voltage) must be enabled. To select a new accumulator cell by the power multiplexer, all four MOSFETs (Q5/Q6 of the synchronous converter and Q7/Q8 of the high-low selection circuit) must be disabled. After selecting the desired cell, Q7 or Q8 is switched on (depending on the cell polarity) and then the synchronous converter can be restarted.

The MOSFETs are controlled by the *hilo-Hi* and *hilo-Lo* signals and needs a dead-time of minimum 25.00 µs during the switching process. Since the *hilo-Hi* and *hilo-Lo* are digital signals, this dead-time must be generated by software. Because the two semiconductors Q7/Q8 are controlled statically (no frequency) the power consumption is very low and MOSFETs with a high gate charge Q_G and low R_{DSon} resistance can be used.

The precise 4 mΩ, 2 W shunt resister R69 on the left side in Figure 50 is used to measure the charge respectively discharge current of the accumulator cell (also used for the current closed-loop control of the synchronous converter). On the PCB, a four terminal sensing (Kelvin sensing) is implemented for R69 to obtain high accuracy. A Kelvin sensing is also used for the cell voltage measurement. The two power outputs *P-Line1* and *P-Line2*

Figure 50 – High-low selection



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are connected on the power multiplexer board (Polarfuchs IIa board) directly to the voltage sensing leads *U-line1* and *U-Line2*. So, the voltage drop from the board-to-board connector J3 has no influence on the measurement.

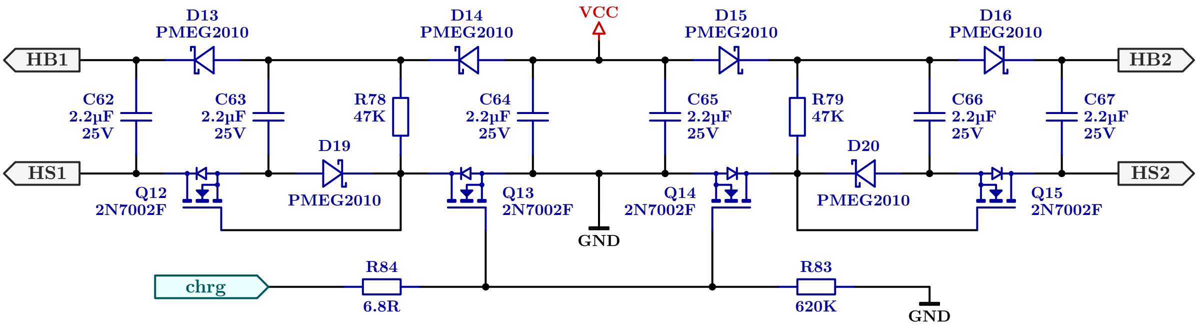
To prevent a cable fire, a 20 A safety fuse (F2) is implemented at the output. This is necessary because the accumulator cell can deliver uncontrolled currents into the circuit if the control fails or the push-pull or synchronous converter stage is damaged. In this case, the fuse - as the weakest link in the circuit - separates the Platinfuchs IIa board from the cell to be balanced. The fuse F2 cannot protect the add-on board Polarfuchs IIa. The digital control system of the Polarfuchs IIa board must always monitor the permitted switching states carefully. Especially when switching to a new cell. But this is a slow process that can be done by software easily (break-test-make functionality).

The resistors R70 and R71 are integrated to test the fuse F2 and the power semiconductors during the start-up process. Depending on the MOSFETs Q5, Q6, Q7 and Q8 switch status, the voltage on *P-Line1* can be monitored and provides information about a triggered fuse and/or the correct function of the MOSFETs.

6.3.4 Double Charge-Pump

While the power supply for the MOSFETs Q6 and Q8 (power supply for the MOSFET drivers) on the low side of the full-bridge is supplied by the ground referenced *VCC* voltage, the high-side power semiconductors Q5 and Q7 needs their own independent supply. To realize a 100 % switch-on time, especially for the high-low selection circuit (half-bridge), the typical bootstrap circuit (charge-pump), where the low side power MOSFETs are used to charge the bootstrap capacitor, is not enough. Therefore, the circuit in Figure 51 generates the two high-side supplies for the MOSFETs Q5 and Q7 (high side power supply for the MOSFET driver U9 and U10). This circuit was specially developed to keep costs down, so only easily available components are used.

Figure 51 – Double charge-pump



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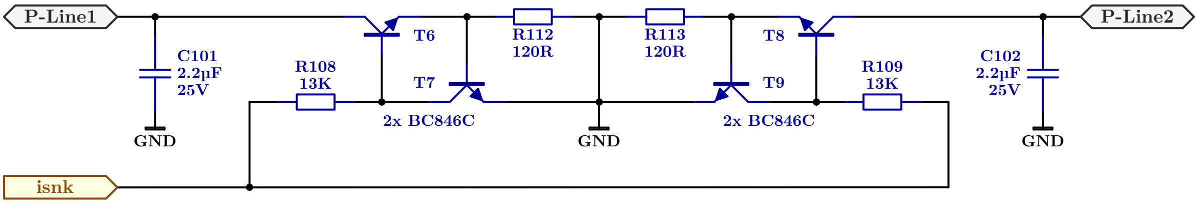
The circuit works like a charge-pump. When the signal *chrg* is high, the switch Q14 is closed (Q15 is open because the gate voltage is negative). The capacitor C66 will be charged by a current flowing over D15, C66, D20 and Q14. After disabling Q14, the switch Q15 will be enabled by the resistor R79 and allows that C66 charges the output capacitor C67, which is the buffer capacitor for the high-side supply. To maintain a permanent energy flow, the *chrg* signal must be fed with a 24 kHz square wave signal (duty cycle = 0.5). The left side of the circuit from Figure 51 shifts the energy in the same way as the one described on the right. Since the left and right sides are independent, the output voltages can have a different reference potential (*HS1* and *HS2*) and thus reliably supplies the high sides of the full-bridge electronic.

6.3.5 Current-Sink Circuit

To test the full-bridge stage at start-up, two current sources are integrated in the printed circuit board. The current sink circuit from Figure 52 tries to pull both power lines *P-Line1* and *P-Line2* to ground when the *isnk* signal is high (4...7 mA). This circuit can also be used to test the Polarfuchs IIa multiplexer board. If the current source circuit is enabled, the full-bridge is disabled and an accumulator cell is selected (two switches of the multiplexer are closed), the difference voltage on *U-Line1* and *U-Line2* (respectively *P-Line1* and *P-Line2*) will be equal to the cell voltage (typical > 1.00 V). If none or only one multiplexer switch (bidirectional power switch) is closed, the voltage should be less than 1.00 V.

Figure 52 – Current-sink circuit



Source: by the author

6.4 Measurement System

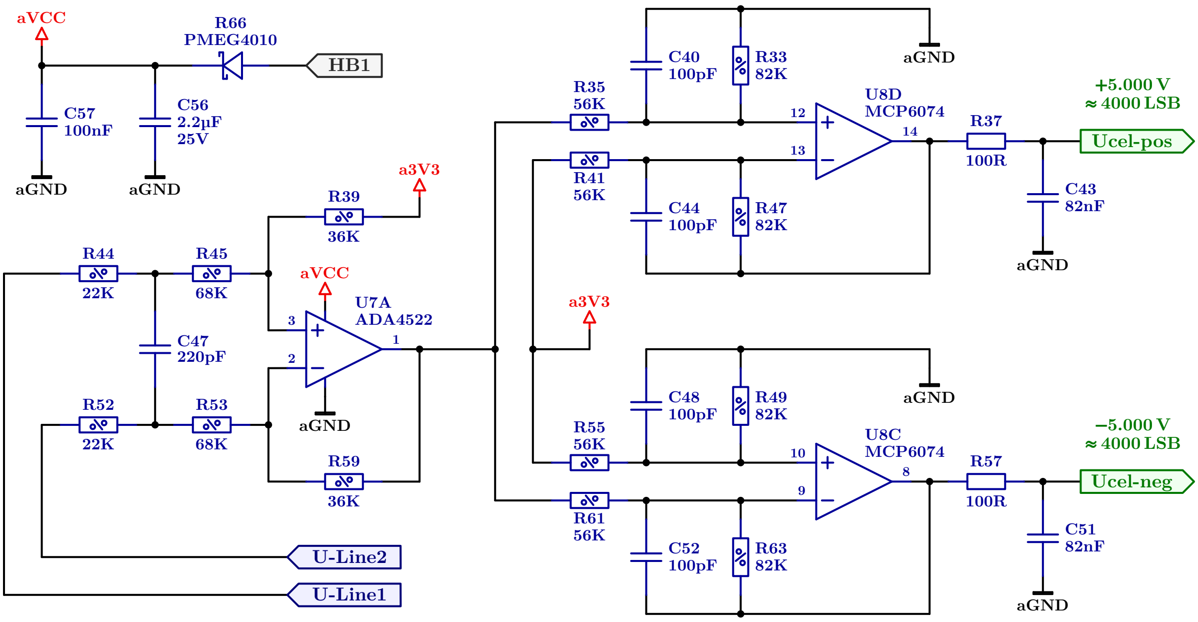
To monitor and control the power transfer from or to the accumulator cell, the digital control system needs all relevant data. Therefore, the analog values must be measured and prepared for the built-in analog-to-digital converter (ADC) of the microcontroller. Depending on the signals and their specific conditions (input range, accuracy, bandwidth etc.) different analog circuits are installed on the board. These circuits are optimized in costs but are also flexible in design, so single parameters like gain and cut-off frequencies can be optimized for the end application.

6.4.1 Cell Voltage Measurement

To measure the accumulator cell voltage U_{Cell} respectively the voltage output of the full-bridge, an analog front-end (AFE) is necessary that adapts the voltage between *U-Line1* and *U-Line2* to the analog input range of the digital control system (ADC input). This amplifier stage must be able to process positive and negative voltages since the full-bridge will generate, depending on the switching status of the multiplexer, also a positive or negative voltage. In addition, the amplifier circuit must transmit the measurement signal true to the original with the smallest error and should also be able to adjust the bandwidth and the amplification factor via hardware. The choice therefore fell on a two-stage operational amplifier circuit, as shown in Figure 53.

The input stage in Figure 53 is a differential amplifier circuit with an input range from *GND* until *VZK* and an amplification factor of 400 mV/V. In doing so, a cell voltage U_{Cell} of maximal ±5000 mV will generate ±2000 mV at pin 1 of the operational amplifier U7A with an offset voltage of 3.30 V to ground. Depending on the polarity, a subsequent differential amplifier takes over the signal, amplifies and references it to *aGND*. If the voltage is positive, U8D will generate the *Ucel-pos* signal (non-inverted signal), else the U8C amplifier will generate *Ucel-neg* (inverted signal). After digitizing both signals, the microcontroller compares it and select the one whose value is greater. In this way, it is possible to obtain a 12-bit resolution (ADC) plus an extra sign bit (in total 13-bit for a range of ±5000 mV). The second amplifier stage uses a gain of 1464.29 mV/V (82 kΩ/56 kΩ). This "crooked" amplification factor was chosen so that at ±5000 mV at the input the

Figure 53 – Cell voltage measurement



Source: by the author

voltage at *Ucel-pos* respectively *Ucel-neg* will be 2928.57 mV. With a voltage reference of 3000 mV and 12-bit resolution of the analog-to-digital converter, this corresponds to a digital value of 4000 LSB (least significant bit).[7] Which give a resolution of 1.25 mV/LSB. The resolution can be further increased utilizing oversampling. For example, 16 measured values can be averaged to increase the resolution to 312.50 µV/LSB.

Due to the integrated capacitors, the circuit has a 3rd order low-pass behavior. The limit frequencies can be calculated according to equation (72), (73) and (74) and must be designed in such a way that aliasing effects are reliably prevented by digitization (anti-aliasing filter). With the values given for resistors and capacitors, the cut-off frequency for all three filter stages is around 20 kHz (±10 %).[8]

$$f_{cut,1} = \frac{1}{4 \cdot \pi \cdot C_{C47} \cdot (R_{R44} \,||\, R_{R45})} = \frac{1}{4 \cdot \pi \cdot 220\,\mathrm{pF} \cdot (22\,\mathrm{k\Omega} \,||\, 68\,\mathrm{k\Omega})} = 21.76\,\mathrm{kHz} \tag{72}$$

$$f_{cut,2} = \frac{1}{2 \cdot \pi \cdot C_{C40} \cdot R_{R33}} = \frac{1}{2 \cdot \pi \cdot 100\,\mathrm{pF} \cdot 82\,\mathrm{k\Omega}} = 19.41\,\mathrm{kHz} \tag{73}$$

$$f_{cut,3} = \frac{1}{2 \cdot \pi \cdot C_{C43} \cdot R_{R37}} = \frac{1}{2 \cdot \pi \cdot 82\,\mathrm{nF} \cdot 100\,\Omega} = 19.41\,\mathrm{kHz} \tag{74}$$

All resistors in Figure 53 with a percent sign (% character) must be high precise resistors with low tolerances and a low-temperature coefficient in order to keep the error small (0.1 %, 25 ppm/K resistors are currently used). Regardless of this, the gain and offset of the voltage measurement channel must be corrected by software, since the analog-to-digital converter of the microcontroller also does not have an ideal transfer characteristic (ADC

[7] The small deviation of −0.381 ‰ can be corrected in the controller using software.
[8] The equations for the inverting amplifier stage are the same as for the non-inverting amplifier.

gain error ±10 LSB; ADC offset error ±5 LSB). Since the input voltage range extends from *GND* to *VZK*, the input voltage range of U7 must at least include ground. To ensure a measurement up to *VZK* potential, the operational amplifier is supplied via the left part of the double charge-pump in Figure 51. The components R66, C56 and C57 in Figure 53 generate therefore the direct voltage *aVCC* that is always at least 5.00 V above the *Out* potential. The operational amplifier ADA4522 used can be substituted by an OPA2182, OP2188 or a similar one with small input voltage offset (important for the current measurement). For U8, an operational amplifier with small offset and a rail-to-rail input and output capability is necessary. The MCP6074 chip can output a voltage close to zero and allows the entire input range of the ADC to be used. The voltage measurement unit only uses commercially available components with standardized housings (footprint), so that subsequent adjustment is easy.

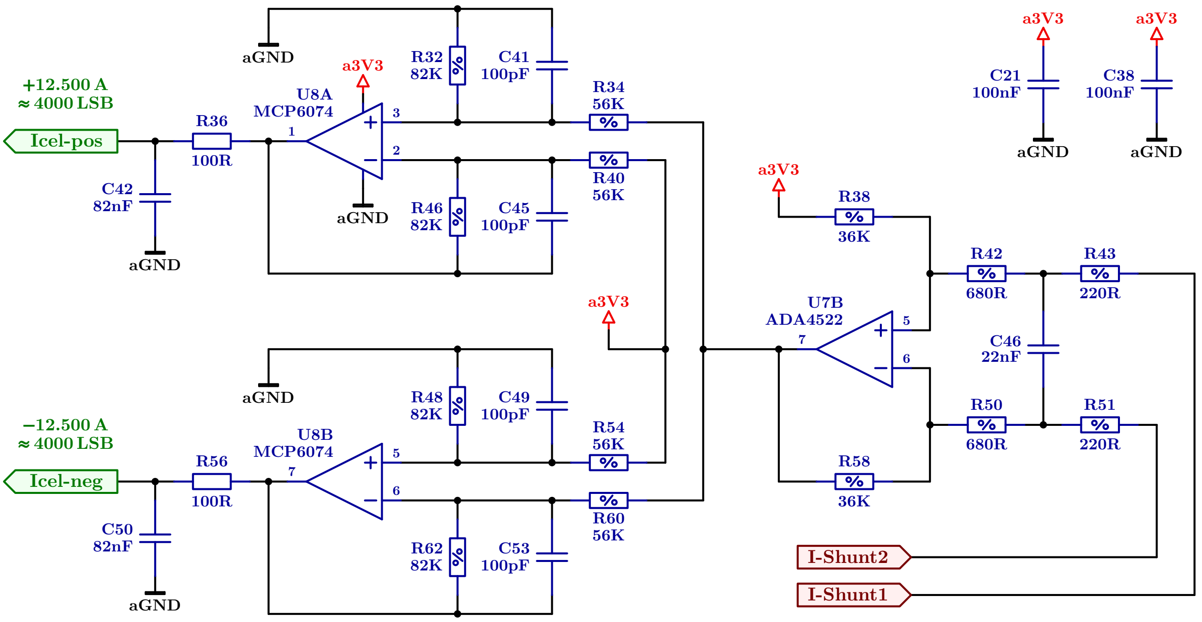
6.4.2 Cell Current Measurement

In order to measure the current with which the accumulator cell is balanced (I_{Cell}), a precise analog front-end stage is necessary. Since the cell can be charged and discharged, this front-end must also be able to process a positive as well as a negative current and adapts the signal to the input range of the digital control system (ADC input). Therefore, a flexible operational amplifier circuit is implemented on the Platinfuchs IIa board.

To measure the current I_{Cell} a shunt resistor is used and generates a voltage drop of maximum ±50.00 mV ($U_{R69} = \pm 12.5\,\mathrm{A} \cdot 4.0\,\mathrm{m\Omega}$). This 4.0 mΩ, 1 % shunt resistor R69 with the two sensing signals *I-Shunt1* and *I-Shunt2* (Kelvin sensing) is described in subsection 6.3.3. Since the potential of *I-Shunt1* can vary between zero and U_{VZK} (since R69 is connected to *Out* of the synchronous converter) the amplifier must work, equal to the cell voltage measurement unit, within this range. Hence, the same circuit is used to amplify the voltage drop of the shunt resistor R69. Figure 54 presents the front-end stage used with the two generated *Icel-pos* and *Icel-neg* signals for the ADC. Since the voltage drop of the resistor is small (maximum ±50.00 mV) the first amplifier stage uses a gain of 40 to increase the signal to ±2.00 V. Because of the small input voltage, the operational amplifier U7 must have an extremely low offset voltage and very low noise. The circuit uses the zero drift operational amplifier ADA4522. This semiconductor has two operational amplifiers in one housing and is so used for the voltage and the current front-ends (please refer subsection 6.4.1). A good replacement with the same footprint and less power consumption will be the OPA2188 operational amplifier.

By the given values for the resistors, the whole circuit will have a transfer factor of 2342.86 mV/A. After digitization, this corresponds to a value of 4000 LSB at a maximum current of 12.50 A (3.125 mA/LSB resolution). The cut-off frequencies of the filters are chosen to be the same as the voltage measurement stage (≈20 kHz) so in a mathematical calculation no phase delay between current and voltage must be considered. The cut-off

Figure 54 – Cell current measurement



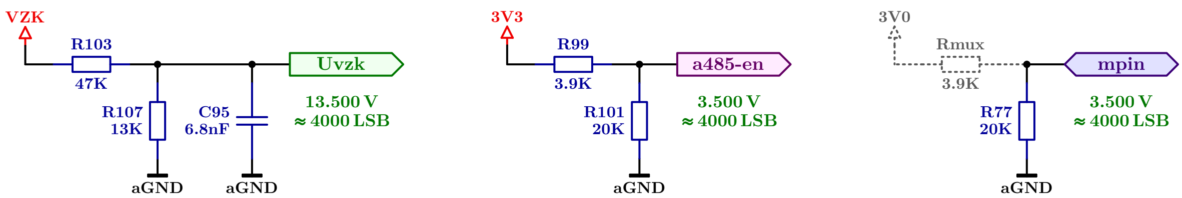
Source: by the author

frequencies can calculate using the equation (72), (73) and (74) after adjusting the values (equation (72)). Due to the 1.00 % tolerance of the shunt resistor R69 and the non-ideal ADC, a software-based correction of gain and offset is necessary to archive high precision.

6.4.3 DC-Link Voltage and Additional Measurements

To measure the *VZK* DC-link potential, a voltage divider is mount on the Platinfuchs IIa board, where the transfer factor is 4000 LSB/35.00 V. The left side of Figure 55 presents this divider (R103 and R107) with the low pass filter capacitor C95 (2.30 kHz cut-off frequency). Because the push-pull converter uses a fix transfer ratio, the measurement of U_{VZK} also represents the **VZK** voltage and accordingly the +12 V main supply.[9] By measuring U_{VZK} over- and under-voltage limits can be defined, and the digital control algorithm can decide to reduce or switch of the transferred power or, if it is really needfully, to disable the whole balancer unit. This is necessary if the discharge energy from the accumulator cell cannot be transferred to the +12 V main supply.

Figure 55 – DC-link voltage and additional measurements



Source: by the author

[9] Due to the voltage drop of the transformer a small error will appear for U_{*VZK*}.

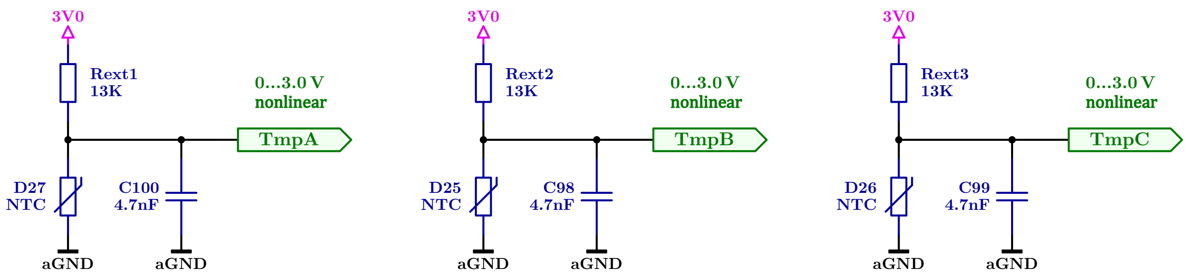
The voltage divider in the middle of Figure 55 allows measuring the voltage of the 3.3 V auxiliary supply on the secondary side (4000 LSB corresponds to 3.50 V). With the current monitor circuit, the absorbed power can be calculated or over- and under-voltage limits can be supervised. To carry out this measurement, a microcontroller with corresponding analog input must be used (dsPIC33EP128GM304) and the controller pin must be reconfigured, since the voltage divider shares the *a485-en* signal with the EIA-485 interface.

The right side of Figure 55 shows also a voltage divider to monitor the switchable 3.0 V supply (4000 LSB/3.50 V). The voltage divider differs from the other two circuits in that the resistor Rmux is not located on the DC/DC converter board, but on the multiplexer board (Polarfuchs IIa). Only after connecting both boards together, the signal *mpin* will show a positive voltage (controller pin configured as input). Depending on the software of the multiplexer board, a different function can also be assigned to the Multipin (*mpin*). For example, a PWM signal can be generated and transmitted to transmit a measured analog signal independently of the I^2C communication to the main controller.

6.4.4 On-Board Temperature Measurement

The DC/DC converter uses three thermistors to measure the temperatures on critical points on the board. The NTC (negative temperature coefficient) sensor D27 is mount on the backside of the PCB near the shunt resistor R69 and the current/voltage amplifier U7. The temperature signal from this sensor can be used to correct the current measurement signals *Icel-pos* and *Icel-neg*. This can be necessary because the 4 mΩ shunt resistor has a tolerance of 1.00 % and a temperature coefficient of 75 ppm/K.[10] The sensors D25, near to the power MOSFETs Q3/Q4, and D26, near to the full-bridge MOSFETs, allows switching of or to reduce the transferred power if the electronic overheat.

Figure 56 – On-board temperature measurement



Source: by the author

As can be seen in Figure 56 the thermistors and the resistors Rext1, Rext2 and Rext3 forms a voltage divider.[11] The capacitors C98, C99 and C100 suppress interferences and noise, generated by fast switching processes. The generated analog signal can be

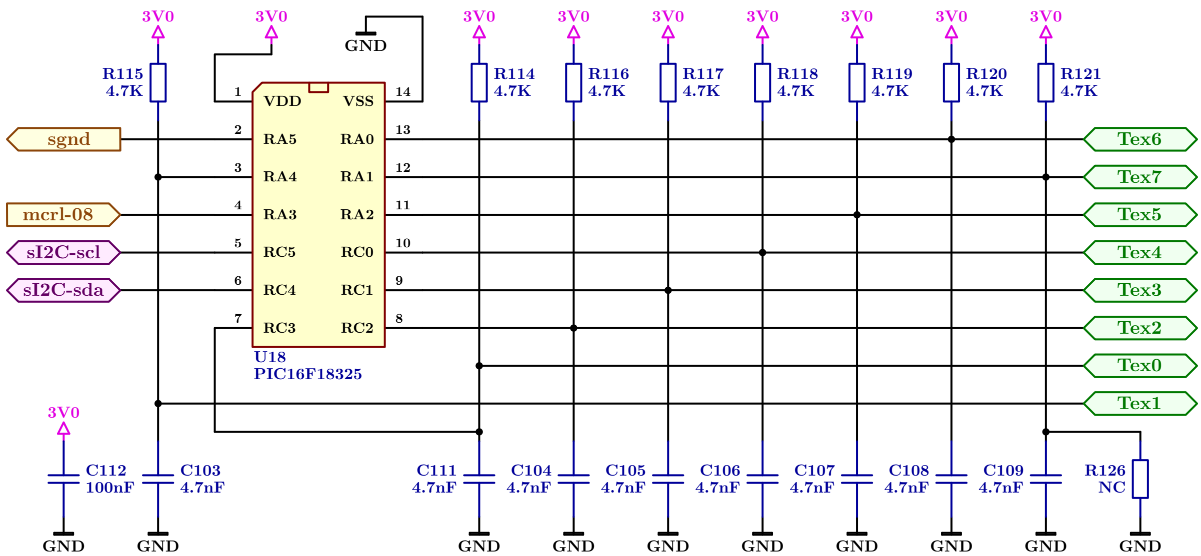
[10] It also allows conclusions to be drawn about the temperature of the power inductor L3.
[11] Rext1, Rext2 and Rext3 are not in the layout and must mount extra on the board → layout respectively design error.

digitized by the ADC of the microcontroller, if the chosen controller has enough analog inputs (dsPIC33EP128GM304). Otherwise, a temperature monitoring is not possible (dsPIC33EP32MC204). Because the output voltage of the divider is strongly non-linear, the microcontroller must linearize the *TmpA*, *TmpB* and *TmpC* signals to get the correct temperatures. This can be done by software by using a lookup-table (LUT) and a simple interpolation calculation.

6.4.5 External Temperature Measurement

For the user (or a higher level control) and the balancing process, the actual temperature of the battery stack is from interest. To reduce effort and costs, sensors are only installed at critical points. Therefore, the Platinfuchs IIa board allows sensing up to eight external temperatures. To realize an easy and inexpensive temperature measurement unit, a small 8-bit microcontroller (Figure 57) is implemented. The PIC16F18325 digitize the analog sensor signals, linearizes and calculates the actual temperatures and makes it available for the main microcontroller (master). Both controllers communicate with each other over an I^2C bus system. The necessary I^2C address for the slave (U18) is thus set by software. The simple connection to the system allows the entire temperature measuring unit to be omitted - if no temperature measuring is required (reduces costs).

Figure 57 – External temperature measurement



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The eight analog inputs (*Tex0* - *Tex7*) uses 4.7 kΩ pull-up resistors (R114 - R121) to form a voltage divider with the external sensors. To suppress interferences received by the sensor leads, 4.7 nF capacitors are integrated on the board. The circuit is optimized for NTC thermistors (actual sensor type: Vishay-NTC 10 KΩ NTCLE100E3103HBO), but can also be used with other sensors like PTCs, RTDs or diodes. For this purpose, resistors and capacitors must be adapted to the used sensor element. Because the characteristic curve of a thermistor is strongly nonlinear and depends on the component specification, the controller needs a lookup-table (LUT) with the appropriate values to determine the actual temperature (preferable with minimum 64 entries). Intermediate values can be calculated by using interpolation.

The thermistors are not directly connected to *GND*. To save energy, the ground used for the sensors can be switched off and is controlled by the *sgnd* signal (Figure 57 and Figure 71). A low signal on *sgnd* disables the ground so that no current can flow over the voltage divider. To measure the temperatures the ground has to be activated and, after the filter capacitors are charged (worst case: $7 \cdot 4.7\,\mathrm{k\Omega} \cdot 4.7\,\mathrm{nF} \approx 160\,\mathrm{\mu s}$) the analog value can be digitized. Since the temperature of an accumulator cell will change slowly, this can be done as an example for all 250 ms (four values per second). Therefore, the simple and cheap PIC16F18325 microcontroller is sufficient to calculate the temperature and handle the communication with the main controller.

If no temperature measurement of the cells are necessary, the sensor pins *Tex0* to *Tex7* can also be used like a port extension with freely selectable functionality. So other electronic modules can be connected to the Platinfuchs IIa board. A full overview of all signals from or to the PIC16F18325 controller, also with their second function, are shown in Table 10.

Table 10 – External temperature measurement - 1st and 2nd functions

Maier, 28 June 2021

Platinfuchs IIa board

	External Temperature Measurement - 1st funktion					PIC16F18325		
#	**label name**	**description**	**comment**	**signal**	**resistor**	**module**	**name**	**pin**
1	*Tex0*	external temperature 0	NTC sensor → nonlinear → software correction	0...3.0 V	4.7 k pull-up	ADC	ANC3	7
2	*Tex1*	external temperature 1	NTC sensor → nonlinear → software correction	0...3.0 V	4.7 k pull-up	ADC	ANA4	3
3	*Tex2*	external temperature 2	NTC sensor → nonlinear → software correction	0...3.0 V	4.7 k pull-up	ADC	ANC2	8
4	*Tex3*	external temperature 3	NTC sensor → nonlinear → software correction	0...3.0 V	4.7 k pull-up	ADC	ANC1	9
5	*Tex4*	external temperature 4	NTC sensor → nonlinear → software correction	0...3.0 V	4.7 k pull-up	ADC	ANC0	10
6	*Tex5*	external temperature 5	NTC sensor → nonlinear → software correction	0...3.0 V	4.7 k pull-up	ADC	ANA2	11
7	*Tex6*	external temperature 6	NTC sensor → nonlinear → software correction	0...3.0 V	4.7 k pull-up	ADC	ANA0	13
8	*Tex7*	external temperature 7	NTC sensor → nonlinear → software correction	0...3.0 V	4.7 k pull-up	ADC	ANA1	12
9	*mcrl-08*	PIC16 master clear pin reset	not used from HW; reset by POR, BOR or Software	low active	3.9 k pull-up	RESET	MCRL	4
10	*sI2C-scl*	synchron I2C clock	I2C communication with...	low active	3.9 k pull-up	I2C1	SCL1	5
11	*sI2C-sda*	synchron I2C data	...the main-microcontroller	low active	3.9 k pull-up	I2C1	SDA1	6
12	*sgnd*	ground for sensor	high → NTC sensors are active (low solves energy)	high active	620 k p-down	I/O	RA5	2
13	*3V0*	3.0 V supply, switchable	3.0 V LDO regulator, LDO disable → RESET	3.0 V; ±3 %	-	POWER	VDD	1
14	*GND*	ground		GND	-	POWER	VSS	14

	External Temperature Measurement - 2nd funktion					PIC16F18325		
#	**label name**	**description**	**comment**	**signal**	**resistor**	**module**	**name**	**pin**
1		external port of Platinfuchs IIa	RC3 / C1IN3- / C2IN3- / IOC / etc.	digital/analog	selectable	?	RC3	7
2		external port of Platinfuchs IIa	RA4 / SOSCO / IOC / CLKOUT / OSC2 / etc.	digital/analog	selectable	?	RA4	3
3		external port of Platinfuchs IIa	RC2 / C1IN2- / C2IN2- / IOC / etc.	digital/analog	selectable	?	RC2	8
4		external port of Platinfuchs IIa	RC1 / C1IN1- / C2IN1- / IOC / etc.	digital/analog	selectable	?	RC1	9
5		external port of Platinfuchs IIa	RC0 / C2IN0+ / IOC / etc.	digital/analog	selectable	?	RC0	10
6		external port of Platinfuchs IIa	RA2 / VREF- / DAC1REF- / IOC / etc.	digital/analog	selectable	?	RA2	11
7	*Tex6*	data for programming	only for programming / C1IN0+ / DAC1OUT1	high active	remove R & C	ICSP	ICSPDAT	13
8	*Tex7*	clock for programming	only for programming / VREF+ (volt. divider)	high active	remove R & C	ICSP	ICSPCLK	12
9	*mcrl-08*	VPP voltage for programming	only for programming, generated by Pickit 3	12.0 V max.	3.9 k pull-up	ICSP	VPP	4
10								5
11								6
12								2
13	*3V0*	3.0 V supply, switchable	also positive reference for internal ADC module	3.0 V; ±3.0 %	-	ADC	VDD	1
14	*GND*	ground	also negative reference for internal ADC module	GND	-	ADC	VSS	14

Source: by the author

6.5 Auxiliary Power Supplies

Multiple auxiliary power supplies are required for proper operation of the power stages and the measurement. This low-power supplies powers the MOSFET drivers, the measurement units, the digital control system, the serial interfaces and, finally, the attachment board Polarfuchs IIa. Because of the potential separation, different power supplies on the primary and secondary side of the Platinfuchs IIa board are implemented.

6.5.1 3.3 V and 7.5 V Supplies

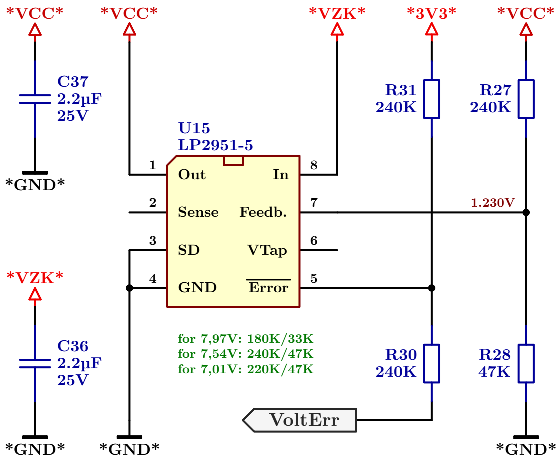
On the primary side of the DC/DC converter board, two auxiliary power-supplies are installed. A low drop-out regulator (Figure 58) generates the **VCC** voltage to power the gate driver U12. The desired output voltage U_{*VCC*} can be adjusted via the resistor divider R27/R28 and must be matched to the MOSFETs Q1 and Q2. For the MOSFETs PSMN3R3-40YS, an output voltage of 7.50 V is set. This allows to switch-on the MOSFETs safely and, at the same time, reduces the necessary power for charging and discharging the MOSFET gates. The output power P_{*VCC*} of the LDO regulator strongly depends on the MOSFET type ($Q_{G,Q1/Q2}$) and the selected driver voltage and increases linearly with the switching frequency. With the self-consumption of the gate driver U12, the power can be calculated as indicated in equation (75).

$$\begin{aligned} P_{*VCC*} &= 2 \cdot f_{sw} \cdot U_{*VCC*} \cdot \left(Q_{G,Q1/Q2}(U_{GS} = U_{*VCC*}) \right) + U_{*VCC*} \cdot I_{op,U12} \\ &= 2 \cdot 120\,\text{kHz} \cdot 7.50\,\text{V} \cdot 38.0\,\text{nC} + 7.50\,\text{V} \cdot 2.00\,\text{mA} \\ &= 83.40\,\text{mW} \end{aligned} \tag{75}$$

The calculation shows that only a small amount of energy is required to control the two MOSFETs Q1 and Q2, even at a switching frequency f_{sw} of 120 kHz. For this reason, an inexpensive low drop-out regulator (LP2951) is sufficient to generate the **VCC** voltage. Due to the higher voltage on **VZK** the LDO regulator consumes approximately 135 mW at the input. The LP2951 chip (U15 in Figure 58) also generates an error signal *VoltErr*, if the input voltage **VZK** is too low to regulate the set output voltage. This error signal is low active and transferred to the secondary side of the Platinfuchs IIa board.

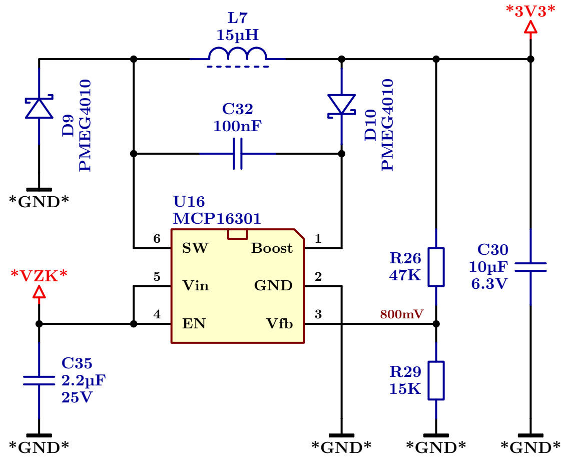
A second 3.3 V supply powers mainly the digital isolator SI8051BD-B-IS (U13) and the EIA-485 serial interface. Due to of the two 120 Ω termination resistors of the EIA-485 bus (necessary to prevent signal reflections), the whole current consumption can be up to 60.00 mA. Therefore, a buck converter is implemented to avoid unnecessary losses. The circuit in Figure 59 uses an integrated step-down regulator (MCP16301) and easily available discrete components to archive a small and cost-effective solution. The converter is powered directly from the **VZK** voltage and generates a constant 3.30 V output voltage with low deviation (maximum ±3 %). The small tolerance also allows using this voltage as a reference for the window comparator of the Autostart circuit.

Figure 58 – 7.5 V auxiliary supply



Source: by the author

Figure 59 – 3.3 V auxiliary supply



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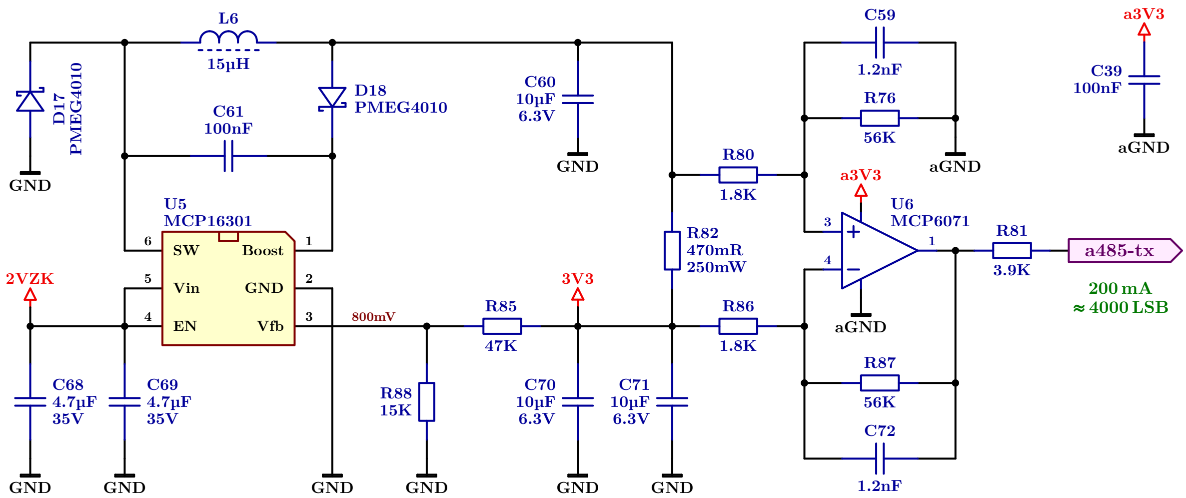
6.5.2 3.3 V Supply with Current Monitoring

The same step-down regulator circuit from the primary side with the MCP16301 chip is also installed on the secondary side of the Platinfuchs IIa board and produces 3.30 V to supply the digital control and peripheral systems. To work also at very low voltages on the 12 V main input (important at the start-up process) the *2VZK* potential is used for the converter input. This *2VZK* voltage is generated by diodes D4/D5 (Figure 40) and is twice the value of *VZK*. Because of the higher output current and to keep the voltage ripple for the digital control system low, the buck-converter from Figure 60 are built up with three output capacitors (C60, C70 and C71) with a total capacity of 30 µF.

Figure 60 – 3.3 V auxiliary supply with current monitoring



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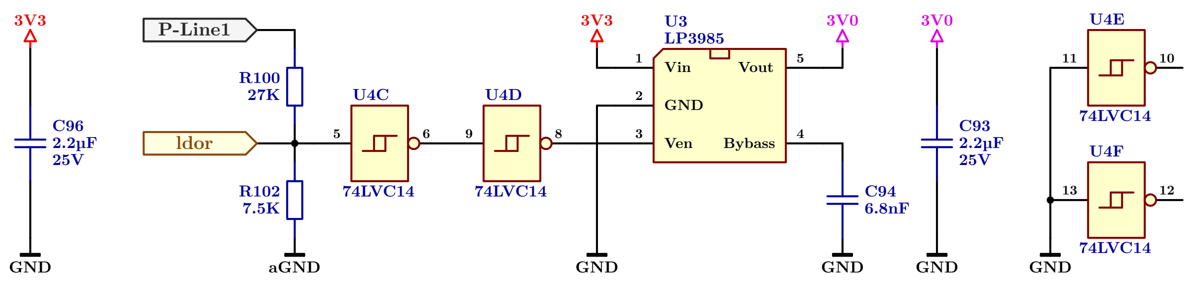
This 3.3 V auxiliary supply powers the microcontroller and all peripherals on the secondary side (with exception to the VDD converter). The output power depends on the current operating status of the individual peripheral modules and reaches values of typically 160 mA (which corresponds to 530 mW). To measure the current consumption, a 470 mΩ shunt resistor (R82) and a difference amplifier are installed. If the microcontroller switches a peripheral circuit on/off or vary some operating conditions, the controller can check the correct function of the module by monitoring the current change. This current amplifier must not be very precise, since only the change in current (before and after a variation) is of interest. Higher accuracy can be achieved by using 0.1 % resistors for R76, R80, R82, R86 and R87, but this will also increase the costs.

Since the microcontroller used does not have enough input pins, the output of the current amplifier uses the same pin as the transmit signal of the EIA-485 serial interface (*a485-tx* signal). To measure the current of the 3.3 V auxiliary supply, the controller has to remap the internal peripheral via software (analog input for *a485-tx*). With the specified component values in Figure 60 the transmission factor (gain) of the current amplifier is 2924.444 mV/200 mA (4000 LSB/200 mA). This is also the maximum current that can be measured.

6.5.3 Switchable 3.0 V Supply

On the secondary side, there is also a 3.0 V low drop-out regulator (U3 in Figure 61). It is powered from the 3.3 V auxiliary supply and takes on several tasks. First, this LDO regulator supplies several peripherals like the onboard temperature sensors, the read-only memory (EEPROM), the circuit to measure external temperatures and the power multiplexer board Polarfuchs IIa. Second, the small tolerance of maximum ±3.0 % of the 3.00 V output allows using the low drop-out regulator as a low-cost voltage reference. The analog-to-digital converter on the Polarfuchs IIa board relates all analog measurements to this reference.

Figure 61 – Switchable 3.0 V auxiliary supply



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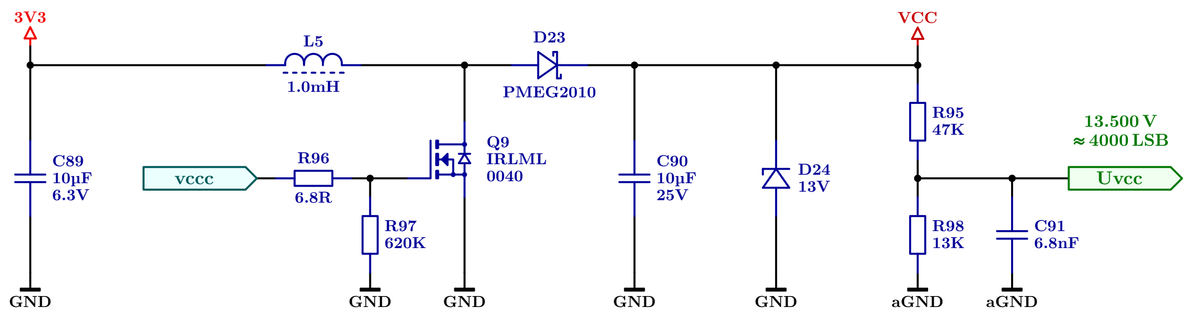
Third, the LDO regulator can generate a hardware reset for the EEPROM, the temperature measure unit and the Polarfuchs IIa add-on board by disabling the energy of these modules. This, if necessary, resets a blocked I^{2}C communication. Disabling also helps to reduce energy in standby mode (disables peripherals). To switch-off (reset) the LP3985im5-3.0 regulator, the controller sets the *ldor* signal low. The *ldor* signal can also be reconfigured to measure the voltage of *P-Line2* (4000 LSB/13.50 V). Therefore, a simple voltage divider (R100 and R102) and two CMOS buffers (U4C and U4D) completes the circuit in Figure 61.

6.5.4 VCC Converter

The 3.3 V supply delivers not enough voltage to control the power MOSFETs on the secondary side. Even logic-level MOSFETs need at least 5.00 V to turn on safely. For this reason, a boost respectively step-up converter (Figure 62) is implemented on the DC/DC converter board Platinfuchs IIa to generate U_{VCC}. This voltage supplies the gate driver U11 for the MOSFETs Q3 and Q4 of the push-pull converter and the half-bridge gate driver U9 and U10 with the MOSFETs Q5/Q6 and Q7/Q8 of the full-bridge system. To ensure that the drivers are adequately supplied and do not switch off due to under-voltage, the converter must produce a minimum voltage of 6.00 V for U_{VCC}. This voltage is sufficient when using logic-level MOSFETs. For standard MOSFETs, with higher threshold-voltages, the *VCC* voltage must be higher and should carefully match to the six MOSFETs used. A higher *VCC* voltage can also reduce the R_{DSon} resistance of logic-level MOSFETs and consequently reduce the power losses - especially at higher currents ($P_L = I_D^2 \cdot R_{DSon}$). Hence, U_{VCC} can be set by the microcontroller depending on the actual operating point.[12]

Figure 62 – VCC boost converter



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The output power P_{VCC} strongly depends on the MOSFET types used for Q3/Q4 and Q5/Q6 and the selected *VCC* voltage (driver voltage) and increases linearly with the switching frequency f_{sw}. The power MOSFETs Q7 and Q8 has no influence, since they are operated statically (no frequency). In addition, the self-consumption of the drivers and a small part of energy for the measurement unit (U7) is necessary. At a driver voltage of 6.00 V P_{VCC} can be roughly calculated as indicated in equation (76). With an estimated efficiency of 75 % for the converter, the power consumption from the 3.3 V supply is around 160 mW.

[12] This function is currently not implemented in software.

$$
\begin{aligned}
P_{VCC} &= 2 \cdot f_{sw} \cdot U_{VCC} \cdot \Big(Q_{G,Q3/Q4}(U_{GS}=U_{VCC}) + Q_{G,Q5/Q6}(U_{GS}=U_{VCC})\Big) \\
&\quad + U_{VCC} \cdot \Big(I_{op(U7)} + I_{op(U9)} + I_{op(U10)} + I_{op(U11)}\Big) + U_{VZK} \cdot I_{op(U7)} \\
&= 2 \cdot 120\,\mathrm{kHz} \cdot 6.00\,\mathrm{V} \cdot \Big(22.0\,\mathrm{nC} + 22.0\,\mathrm{nC}\Big) \\
&\quad + 6.00\,\mathrm{V} \cdot \Big(2.00\,\mathrm{mA} + 1.20\,\mathrm{mA} + 1.20\,\mathrm{mA} + 2.00\,\mathrm{mA}\Big) + 8.57\,\mathrm{V} \cdot 2.00\,\mathrm{mA} \\
&= 118.90\,\mathrm{mW}
\end{aligned}
\tag{76}
$$

P_{VCC} increases to 323.34 mW, if the digital control system sets an output voltage of 12 V (input power consumption around 430 mW). This corresponds to the maximum of 131 mA on the output of the 3.3 V supply. To monitor the real current consumption, the difference amplifier of the 3.3 V supply system delivers a current proportional output signal (please refer subsection 6.5.2).

The combination of a buck converter followed by a boost converter allows generating a fixed U_{VCC} voltage in the range from approximately 5.00 V to 13.00 V, independently of the *VZK* potential. Another advantage is the simple connection between the microcontroller and the ground connected switching MOSFET Q9. If the MOSFET is carefully selected (IRLML0040), the 3.30 V supply of the digital control system is sufficient to switch on Q9 safely. To save costs, a separate step-up regulator chip was dispensed with. The required 24 kHz PWM signal is generated by the microcontroller, and the feedback control (closed-loop control) is realized by an algorithm in the controller. The resistor divider R95/R98 to measure the output voltage has a transmission factor of 2925.000 mV/13.5 V (4000 LSB/13.5 V) with a cut-off frequency of 2.30 kHz.

6.5.5 VDD Converter

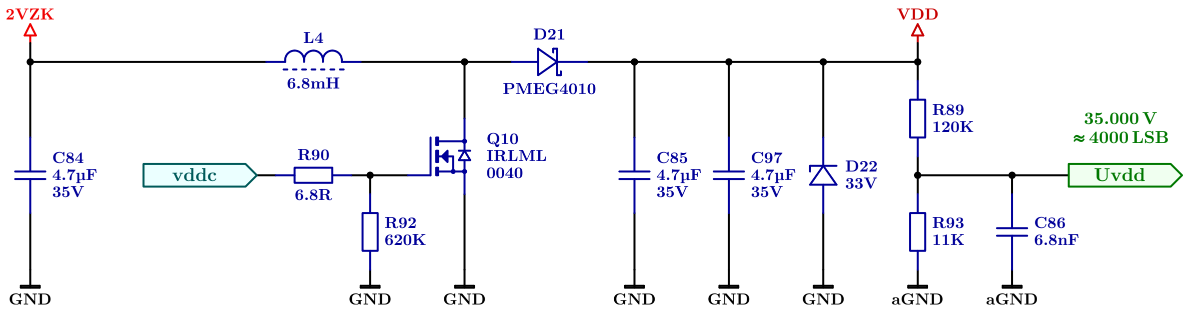
In addition to the switchable 3.0 V supply, the board Polarfuchs IIa needs a second auxiliary supply (*VDD*). This supply powers all bidirectional power-switches on the attachment board with a voltage in the range from 20.00 V to maximal 33.00 V. The optimal voltage and the current consumption depends on the components and circuits used on the multiplexer board Polarfuchs IIa. Typical values for the output voltage and current on *VDD* are 28.00 V and around 1.50 mA per switch. Therefore, the output power P_{VDD} can be calculated as indicated in equation 77. With an estimated efficiency of 70 % the power consumption will be approximately 120 mW.

$$P_{VDD} = 2 \cdot I_{Switch} \cdot U_{VDD} = 2 \cdot 1.50\,\mathrm{mA} \cdot 28.00\,\mathrm{V} = 84.00\,\mathrm{mW} \tag{77}$$

The *VDD* potential is the highest voltage in the system. Therefore, a boost converter is necessary to generate this voltage. Similar to the circuit from subsection 6.5.4 the *VDD* converter uses a discrete circuit with a ground connected MOSFET (Figure 63) and a resistor divider for the analog feedback signal (transmission factor: 2938.931 mV/35.0 V or

4000 LSB/35.0 V; cut-off frequency: 2.30 kHz). The 24 kHz PWM signal and the feedback control (digital closed-loop control) are realized in the microcontroller.

Figure 63 – VDD boost converter



Source: by the author

The *VDD* auxiliary supply is fed from the *2VZK* voltage that is supplied by the secondary side of the push-pull converter (subsection 6.2.1). Therefore, current monitoring with the difference amplifier (Figure 60) is not possible. But regardless of that, the output current from *VDD* is measured on the add-on board Polarfuchs IIa. With a maximum output current of 5.00 mA at 30.0 V and an estimated efficiency of 70 % the VDD supply requires maximal 215 mW input power.

6.6 Digital Control System

Independently of the power output range, every DC/DC converter needs an appropriate control. This can be implemented as an analog circuit (specialized semiconductor) or processed as an algorithm within a microprocessor. On the Platinfuchs IIa printed circuit board, a cost optimized digital control system manages all measure and control signals. With the peripheral electronic, this digital control system forms an embedded system that must be fast enough to calculate an appropriate response for the specific hardware based on the measurements (real-time requirement).

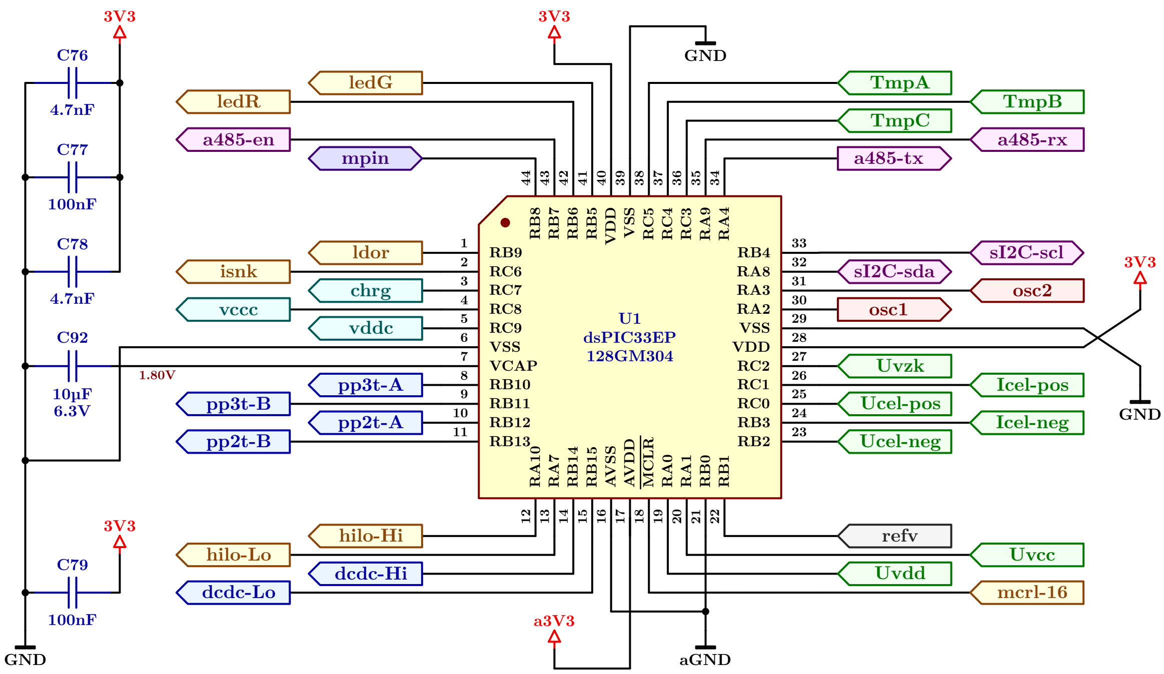
6.6.1 16-bit Microcontroller

The main part of the digital control system is a high integrated 16-bit microcontroller from Microchip Technology Inc. The semiconductor chip dsPIC33EP128GM304 works with up to 70 MIPS (million-instructions-per-second) and has an internal digital-signal-processing engine to increase data throughput. Numerous peripheral modules like timers, direct-memory-access, analog-to-digital converter (ADC), high speed PWM pairs, communication interfaces etc. are also integrated and works without blocking the central processing unit.

The controller was chosen because of the fast and accurate 12-bit internal ADC ($INL = \pm 3.0$ LSB and $DNL = \pm 1.0$ LSB) and the 44 lead plastic TQFP. With 800 µm contact pitch, the controller can be mounted on a PCB with a cooper layer up to 105 µm. A printed circuit board with more cooper will increase heat transfer and reduce the power losses of the energy conversion ($P_L = I^2 \cdot R_{Cu}$). The dsPIC33EP128GM304 chip is pin compatible with several other controllers from the same series. So, the digital control system can optimize in function and/or costs.[13]

Because of the small numbers of pins (reduced costs), all pins of the microcontroller are used. The power connections (with some decoupling capacitors) and the analog/digital signals with their label names are shown in Figure 64. Each connection has a special function, which is specified by the corresponding hardware. Some pins have two functions and works like an input or an output. To select the 2nd-function, the controller has to remap the internal peripheral structure for the desired pin. A full overview of all signals from or to the microcontroller and their label names are shown in Table 11 and Table 12.

Figure 64 – 16-bit dsPIC33EP128GM304 microcontroller



Source: by the author

6.6.2 Clock Generation and Non-Volatile Memory

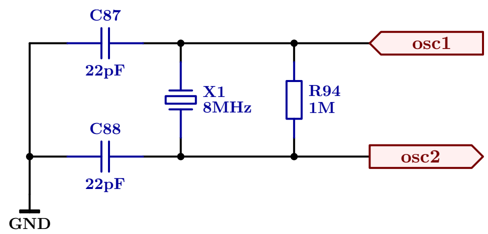
Although the controller dsPIC33EP128GM304 (Figure 64) has a clock management with an internal fast RC oscillator with ±2.0 % accuracy, an extra 8.00 MHz quartz is mount on the board to generate a precise time-base for the microcontroller (Figure 65). This accurate clock is intended for the serial EIA-485 interface (< ±1.0 % is needfully) and

[13] As example, the dsPIC33EP32MC204 chips has less memory and less analog inputs, but costs only 1.16 €/piece (5000+) instead of 3.20 €/piece (5000+).

allows calculating the transferred energy to or from the accumulator cell more accurate ($E = U \cdot I \cdot t$).

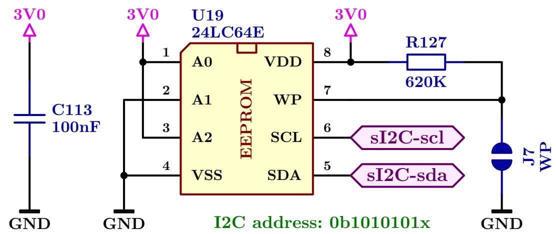
The dsPIC33EP series does not have a non-volatile memory. Calibration values, status/error information, and, especially, cell parameters and their changes over the time cannot be stored. To overcome this disadvantage, a 64 kbit EEPROM is installed on the Polarfuchs IIa board. The 24LC64E semiconductor (U19 in Figure 66) uses the two-wire I^2C bus to communicate with the dsPIC33EP controller and has a write-protect pin (J7) to protect a part of the memory from write operations (ideal for calibration values). The I^2C address is set by hardware (layout) and reads as 0b1010101x.

Figure 65 – 8.0 MHz quartz



Source: by the author

Figure 66 – Non-volatile memory



Source: by the author

6.6.3 I^2C Interface

For communication between the two printed circuit boards Platinfuchs IIa and Polarfuchs IIa as well as for the non-volatile memory and the external temperature measurement unit, an I^2C bus system is used. The synchronous I^2C bus is implemented to reduce pins of the controller and wires on the PCB. Especially due to the use of the I^2C bus for communication between the DC/DC converter and multiplexer board, the costs for the connector could be significantly reduced (only two pins are necessary).

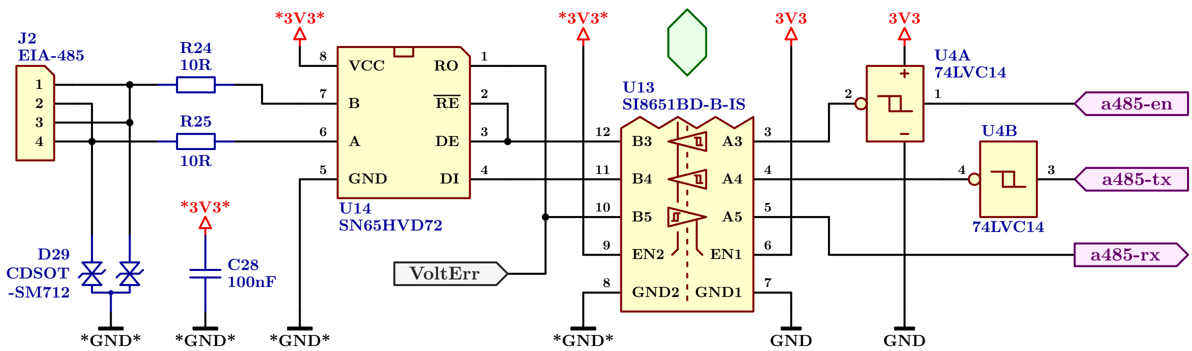
The hardware of the I^2C interface used is simple. Only two pull-up resistors for the lines *sI2C-scl* (clock) and *sI2C-sda* (data) are necessary (R104 and R105 in Figure 70). All other important communication modules are integrated in the appropriate semiconductor chips. Because of the open-drain design, where only the pull-up resistors generate a high level, the I^2C bus is easy to disturb. Therefore, this bus system is only for short cable length and low data rates. Because of the proximity to the power converter stages, the I^2C interface works only with 120 kbit/s and uses the most significant bit (MSB) of the byte as an odd parity bit. Address assignment, protocol generation and error handling (like parity generation and checking) is a part of the individual software. Only the non-volatile memory uses a fixed state machine with defined protocol and a I^2C address, which is set by hardware (layout) and reads as 0b1010101x.

6.6.4 EIA-485 Interface

For exchange data with other balancer modules or a higher-level control unit, an EIA-485 interface is available on the Platinfuchs IIa board. The asynchronous EIA-485 bus specification uses only two wires to transmit the inverted and non-inverted levels of a one-bit data signal. The differential signal transmission and a common voltage range from −7.00 V to +12.00 V (SC of EIA-485 corresponds to **GND**) enables the EIA-485 bus to achieve a high level of interference immunity over long distances. The easy implementation (only two wires), the low costs and the possibility to connect over 200 devices are other benefits. This half-duplex interface is therefore widely used in industry and a communication protocol like Modbus, PROFIBUS or similar can be used (software dependent).

Figure 67 shows the hardware for the EIA-485 interface. The three signals *a485-rx*, *a485-tx* and *a485-en* are generated respectively processed by an UART module in the dsPIC33EP128GM304 microcontroller. Because of the second function for *a485-tx* and *a485-en*, these two signals are buffered by a logic inverter (inverted signals - important for the controller configuration). All three digital signals are transmitted from/to the secondary side to/from the primary side by the digital isolator SI8051BD-B-IS (U13) and, in combination with the SN65HVD72 semiconductor (U14), produce the differential signal for the EIA-485 bus. Resistor R24 and R25 and the TVS double diode CDSOT23-SM712 (D29) protects U14 from fast transient bursts and electrostatic discharges up to 30 kV. To prevent signal reflection on the bus, two 120 Ω termination resistors on the end of the network are necessary. The SN65HVD72 chip is powered by a 3.30 V supply to reduce the current consumption caused by these two resistors. A fast and especially short communication protocol can also reduce the power consumption by reducing the time to send the message.

Figure 67 – EIA-485 interface

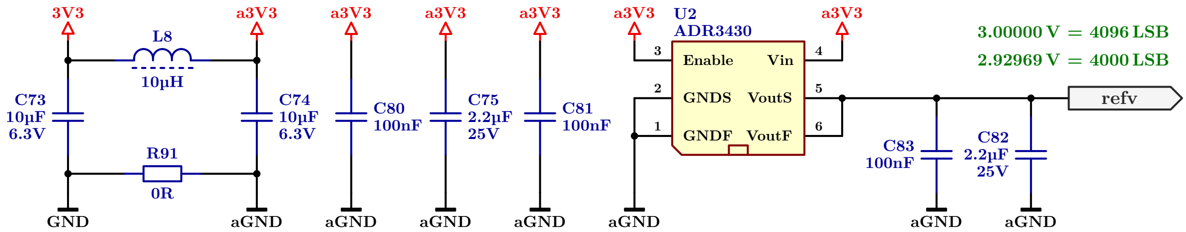


Source: by the author

6.6.5 Voltage Reference

Although numerous of peripheral modules are integrated in the controller, the dsPIC33EP series has no reference voltage module. However, a precise voltage reference is a key element for a correct measurement. The internal ADC module of the controller relates all analog measures to this voltage. A deviation in the reference output voltage inevitably leads to a measurement error. Therefore, on the Platinfuchs IIa board a high accuracy 3.00 V voltage reference (U2 in Figure 68) and several filter capacitors are implemented. With an initial accuracy of ±0.1 % and a maximum temperature coefficient of 8.00 ppm/K the ADR3430 chip is the main reference for the whole system.

Figure 68 – 3.0 V, ±0.1 % voltage reference



Source: by the author

Figure 68 shows also a PI filter realized by C73, C74 and L8. This filter decouples the analog from the digital circuits and thus prevents spikes in the analog measurement, caused by switching operations in the digital part. The 0 Ω resistor R91 (SMD bridge) separates the analog ground (*aGND*) from the digital/power ground (*GND*). The two circuit grids are only connected via this central point near the microcontroller. In this way, no equalizing currents from the power unit can flow via the analog ground and trigger a voltage drop there. A voltage drop in the mV range, caused by constant or pulsed currents in the power section, would lead to undesired offset errors and noise in the measurement signals. If necessary, R91 can be replaced by an inductance (e.g. 1 µH) to minimize capacitive interference. The potentials *a3V3* and *aGND* on the whole board are strictly used for the analog circuit parts to ensure signal integrity.

Table 11 – Digital control system - 1st function

Maier, 28 June 2021

Platinfuchs IIa board

	Digital Control System - 1st function					dsPIC33EP512GM604		
#	**label name**	**description**	**comment**	**signal**	**resistor**	**module**	**name**	**pin**
1	*Icel-pos*	battery-cell current, positive	gain: 2.928571 V / +12.500 A (≈4000 LSB / +12.500 A)	0...3.0 V	-	ADC1	AN7	26
2	*Icel-neg*	battery-cell current, negative	gain: 2.928571 V / -12.500 A (≈4000 LSB / -12.500 A)	0...3.0 V	-	ADC1	AN5	24
3	*Ucel-pos*	battery-cell voltage, positive	gain: 2.928571 V / +5.000 V (≈4000 LSB / +5.000 V)	0...3.0 V	-	ADC1	AN6	25
4	*Ucel-neg*	battery-cell voltage, negative	gain: 2.928571 V / -5.000 V (≈4000 LSB / -5.000 V)	0...3.0 V	-	ADC1	AN4	23
5	*Uvzk*	DC-link voltage	gain: 2.925000 V / +13.500 V (≈4000 LSB / +13.500 V)	0...3.0 V	-	ADC1	AN8	27
6	*Uvcc*	VCC converter voltage	gain: 2.925000 V / +13.500 V (≈4000 LSB / +13.500 V)	0...3.0 V	-	ADC1	AN1	20
7	*Uvdd*	VDD converter voltage	gain: 2.938931 V / +35.000 V (≈4000 LSB / +35.000 V)	0...3.0 V	-	ADC1	AN0	19
8	*TmpC*	buck-boost converter temperature	NTC sensor → nonlinear → software correction	0...3.0 V	-	ADC1	AN29	36
9	*TmpB*	push-pull converter temperature	NTC sensor → nonlinear → software correction	0...3.0 V	-	ADC1	AN30	37
10	*TmpA*	precision-amplifier temperature	NTC sensor → nonlinear → software correction	0...3.0 V	-	ADC1	AN31	38
11	*refv*	3.0 V refernce for ADC	3.0 V ±0.1 % 8 ppm/°C (+2.92969 V = 4000 LSB)	3.0 V; ±0.1 %	-	ADC	VREF+	22
12	*aGND*	analog ground		0.0 V	-	ADC	VREF-	21
13	*a3V3*	3.3 V analog supply		3.3 V; ±3 %	-	ADC	AVDD	17
14	*aGND*	analog ground		0.0 V	-	ADC	AVSS	16
15	*a485-rx*	asynchron EIA-485 receive	hi → 1, lo → 0; TX active → interpret VoltErr	high active	-	UART1	RPI25	35
16	*a485-tx*	asynchron EIA-485 transmit	hi → 0, lo → 1; RX active → interpret curr-amp.	low active	current-amp.	UART1	RP20	34
17	*a485-en*	asynchron EIA-485 enable	lo → TX, hi → RX (+ measure 3.3 V system)	low active	3.9 k pull-up	UART1	RP39	43
18	*sI2C-scl*	synchron I2C clock	I2C interface for add-on board Polarfuchs IIa, and...	low active	3.9 k pull-up	I2C2	SCL2	33
19	*sI2C-sda*	synchron I2C data	...external temperature measure unit and EEPROM	low active	3.9 k pull-up	I2C2	SDA2	32
20	*mpin*	pin with multiple functions	SPI or TCK, ASCL1, T4CLK, OC5, FLT1, etc.	analog/digital	ext. 3.9 k p-up	?	RP40	44
21	*osc1*	8.0 MHz quartz crystal	accurate clock-generator for EIA-485 and...	≈3.0 V Sinus	-	OSC	OSC1	30
22	*osc2*	8.0 MHz quartz crystal	...precise time measurement (for E = U · I · t)	≈3.0 V Sinus	-	OSC	OSC2	31
23	*mcrl-16*	dsPIC master clear pin reset	not used from HW; reset by POR, BOR or Software	low active	3.9 k pull-up	RESET	MCLR	18
24	*ledG*	light emitting diode - green	activates green LED (ca. 2.8 mA)	high active	-	I/O	RB5	41
25	*ledR*	light emitting diode - red	activates red LED (ca. 3.2 mA)	high active	-	I/O	RB6	42
26	*ldor*	3.0 V LDO regulator, switchable	3.0 V supply for add-on board Polarfuchs IIa etc.	high actice	volt.div. Line1	I/O	RB9	1
27	*isnk*	current-sink circuit	current sink for Line1 and Line2; each 4...7 mA	high active	-	I/O	RC6	2
28	*hilo-Hi*	high-low circuit, high side switch	high active → Line2 is VZK (locked with hilo-Lo)	high active	≈240 k p-down	I/O	RA10	12
29	*hilo-Lo*	high-low circuit, low side switch	high active → Line2 is GND (locked with hilo-Hi)	high active	≈240 k p-down	I/O	RA7	13
30	*dcdc-Hi*	buck-boost, high side switch	120 kHz PWM (100...150); 0...100 % ton	high actice	≈240 k p-down	PWM1	PWM1H	14
31	*dcdc-Lo*	buck-boost, low side switch	120 kHz PWM (100...150); 100...0 % ton	high actice	≈240 k p-down	PWM1	PWM1L	15
32	*pp2t-A*	prim. side push-pull, phase A	120 kHz PWM (100...150); 50 % toff, 50 % ton (fix)	high actice	620 k p-down	PWM2	PWM2H	10
33	*pp2t-B*	prim. side push-pull, phase B	120 kHz PWM (100...150); 50 % toff, 50 % ton (fix)	high actice	620 k p-down	PWM2	PWM2L	11
34	*pp3t-A*	sec. side push-pull, phase A	120 kHz PWM (100...150); 50 % toff, 50 % ton (fix)	high actice	620 k p-down	PWM3	PWM3H	8
35	*pp3t-B*	sec. side push pull, phase B	120 kHz PWM (100...150); 50 % toff, 50 % ton (fix)	high actice	620 k p-down	PWM3	PWM3L	9
36	*vccc*	VCC converter (gate driver)	24 kHz PWM (20...50); 0...90 % ton (never 100 %)	high actice	620 k p-down	OC1	RP56	4
37	*vddc*	VDD converter (auxiliary voltage)	24 kHz PWM (20...50); 0...90 % ton (never 100 %)	high actice	620 k p-down	OC2	RP57	5
38	*chrg*	double charge pump	24 kHz PWM (20...50); 50 % toff, 50 % ton (fix)	high actice	620 k p-down	OC3	RP55	3
39	*3V3*	3.3 V supply		3.3 V; ±3 %	-	POWER	VDD	28
40	*3V3*	3.3 V supply		3.3 V; ±3 %	-	POWER	VDD	40
41	*1V8*	1.8 V core voltage	core voltage of dsPIC (internal LDO regulator)	1.8 V	-	POWER	VCAP	7
42	*GND*	ground		GND	-	POWER	VSS	6
43	*GND*	ground		GND	-	POWER	VSS	29
44	*GND*	ground		GND	-	POWER	VSS	39

Source: by the author

Table 12 – Digital control system - 2nd function

Maier, 28 June 2021

Platinfuchs IIa board

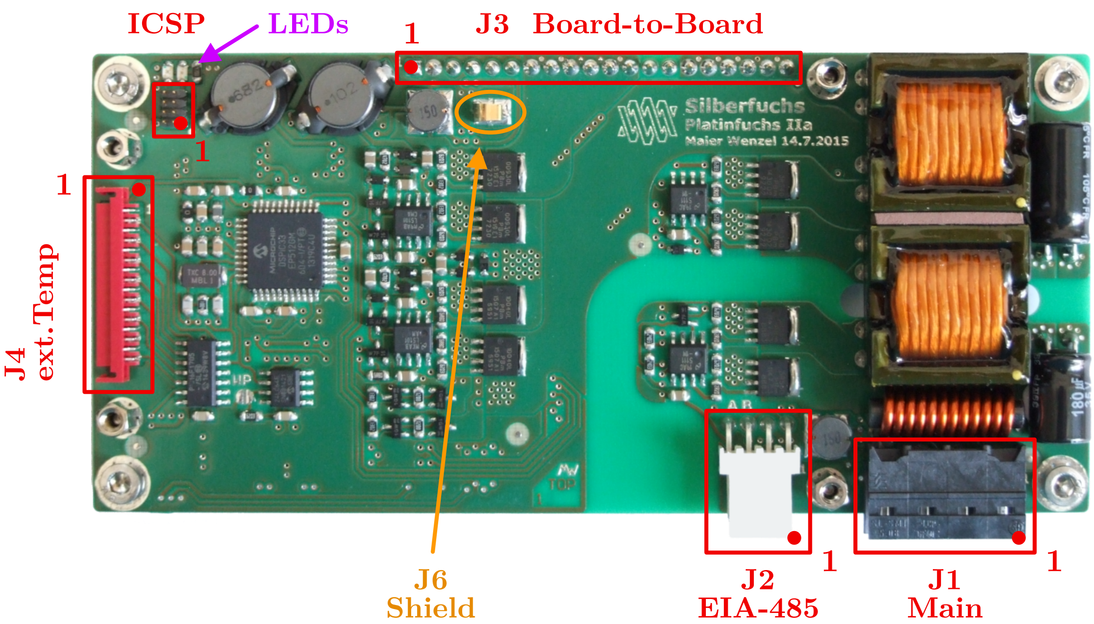
	Digital Control System - 2nd function						dsPIC33EP512GM604		
#	**label name**	**description**	**comment**	**signal**	**resistor**	**module**	**name**	**pin**
1	*Icel-pos*	cell over-current, negative	over-current detection (actual not used)	0...3.0 V	-	CMP3	C3IN1-	26
2	*Icel-neg*	cell over-current, positive	over-current detection (actual not used)	0...3.0 V	-	CMP1	C1IN1-	24
3	*Ucel-pos*	cell under/over-voltage, negative	(under)/over-current detection (actual not used)	0...3.0 V	-	CMP3/4	C4IN4-	25
4	*Ucel-neg*	cell under/over-voltage, positive	(under)/over-current detection (actual not used)	0...3.0 V	-	CMP1/2	C2IN3-	23
5								27
6								20
7	*Uvdd*	VDD under-voltage	under-voltage detection (actual not used)	0...3.0 V	-	CMP5	C5IN2-	19
8								36
9								37
10								38
11								22
12								21
13								17
14								16
15	*a485-rx*	*VCC* undervoltage (VoltErr)	low signal → *VCC* and *VZK* < 7.100 V	low active	-	I/O	RB0	35
16	*a485-tx*	3.3 V supply current-measure	gain: 2.924444 V / +200 mA (≈4000 LSB / +200 mA)	0...3.0 V	-	ADC1	AN24	34
17	*a485-en*	3.3 V supply voltage-measure	gain: 2.92887 V / +3.500 V (≈4000 LSB / +3.500 V)	0...3.0 V	-	ADC1	AN25	43
18								33
19								32
20	*mpin*	3.0 V (ldor) voltage-measure	gain: 2.928870 V / +3.500 V (≈4000 LSB / +3.500 V)	0...3.0 V	need 3.9 k p-up	ADC1	AN26	44
21								30
22								31
23	*mcrl-16*	VPP voltage for programming	only for programming, generated by Pickit 3	12.0 V max.	3.9 k pull-up	ICSP	VPP	18
24	*ledG*	data for programming	only for programming, generated by Pickit 3	high active	-	ICSP	PGED2	41
25	*ledR*	clock for programming	only for programming, generated by Pickit 3	high active	-	ICSP	PGEC2	42
26	*ldor*	P-Line1 voltage-measure	gain: 2.934783 V / +13.500 V (≈4000 LSB / +13.500 V)	0...3.0 V	volt.div. Line1	ADC1	AN27	1
27								2
28								12
29								13
30								14
31								15
32								10
33								11
34								8
35								9
36								4
37								5
38								3
39								28
40								40
41								7
42								6
43								29
44								39

Source: by the author

6.7 Power and Signal Connectors

To connect the Platinfuchs IIa board with power, communication and sensor signals, five connectors are arranged on the board edges (Figure 69). The pin 1 position of each connector is marked on the circuit board as a number or a dot. Incorrect connection of the cables (especially the power supply) can permanently damage the electronic circuit. For the male and female headers, standardized connectors are selected. This allows to find and use different mating connectors to connect the necessary cables to the module. So, an easy and fully pluggable solution for the user is available.

Figure 69 – Connector position on the Platinfuchs IIa board



Source: by the author

6.7.1 +12 V Main Supply Connector

For connecting the Platinfuchs IIa electronic to the +12 V main supply, a standardized 4-pin connector is mount on the PCB (J1 in Figure 39 and Figure 69). The 4-pin, 90° PCB connector OMNIMATE Signal (SL-SMT 5.08HC/04/90 1.5SN BK from Weidmüller GmbH & Co. KG) with a standardized pin pitch of 5.08 mm is compatible with many different mating connectors from the same series. So, the user can select an optimal, fully pluggable solution to connect a cable to the Silberfuchs battery management system. Utilizing four pins for J4, multiple Platinfuchs IIa boards can be connected in a daisy chain configuration. With a maximum power transfer of 45.00 W and a minimum input voltage of 7.50 V the current reaches 6.00 A. Therefore, the cable should have a minimum copper cross-section of 0.50 mm^2. In order to reduce line losses, at least a 1.00 mm^2 cable is recommended.

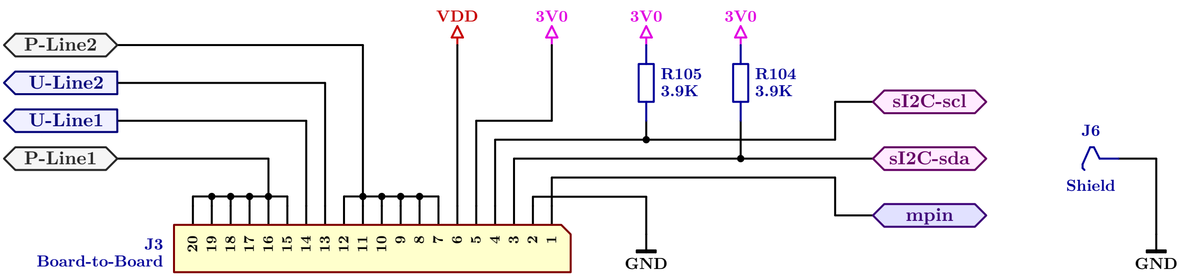
6.7.2 EIA-485 Interface Connector

To connect the serial EIA-485 bus system to the Platinfuchs IIa module, a 90° PCB connector (male header) is available on the board (J2 in Figure 67 and Figure 69). This 2.54 mm wire-to-board header (KK 254 series from Molex LLC) is also implemented with 4-pins to enable a connection in daisy chain configuration. To increase noise immunity, a twisted pair cable for wiring is recommended (however, this does not replace the 120 Ω termination resistors).

6.7.3 Board-to-Board Connector

On the Platinfuchs IIa board there is also a 20-pin, 0° single row pin header with a standardized 2.54 mm pin pitch mount (Figure 69). In combination with the 20-pin female header on the Polarfuchs IIa electronic, a board-to-board connection for power and signals is realized. Figure 70 shows the pinout of this connector. To increase power capability, six pins for *P-Line1* and six pins for *P-Line2* are connected in parallel. The separation of power transfer lines (*P-Line1* / *P-Line2*) and feedback lines (*U-Line1* / *U-Line2*) allows realizing a kelvin connection (four-terminal sensing) on the add-on board. So, the resistance of the connector J3 has no influence at the measurement. To supply and communicate with the Polarfuchs IIa board, only six pins (pin 1 until pin 6) of this connector are used.

Figure 70 – Board-to-board connector



Source: by the author

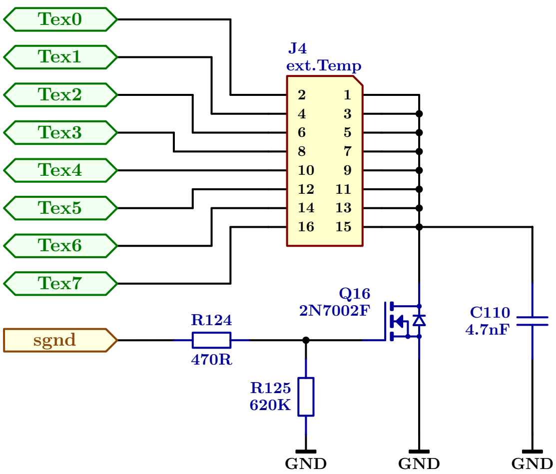
On the right side in Figure 70 a special single pin "connector" (J6) is shown. This spring contact connects the ground potential *GND* to an aluminum profile, which can be mounded between the two printed circuit boards, Platinfuchs IIa and Polarfuchs IIa. This profile (with thermal gap pads), if used, allows spreading the heat of the components and, with the connection to *GND*, is a protection for electromagnetic radiation produced by the converter stages.

6.7.4 External Temperature Sensor Connector

To connect up to eight external temperature sensors like thermistors, a 16-pin, 90° connector is available on the DC/DC converter board (Figure 69). For the connector J4 in Figure 71 a space-saving MicroMatch 1.27 mm contact spacing connector is used

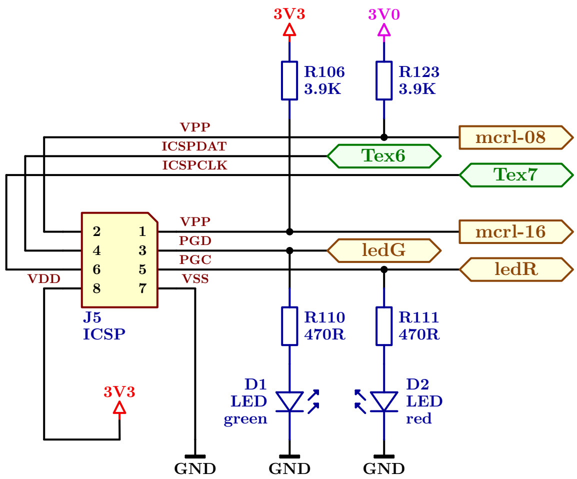
(MicroMatch TMM-5-L-16-1 from Amphenol Corporation). Every temperature sensor can be connected by two wires to the electronic (simplifies wiring). Because the accumulator cells to be measured will have another potential like these sensors (the potential of the electronic changes relative to the cells, depending on the selected cell), the temperature sensors and their wiring need to be safely isolated. The isolation must withstand a voltage of at least 150 V.

Figure 71 – Temp. sensor connector



Source: by the author

Figure 72 – ICSP programming connector



Source: by the author

6.7.5 Programming Connector

For in-circuit programming of the dsPIC33EP128GM304 and the PIC16F18325 microcontrollers, a small connector is mount on the PCB (Figure 69). Figure 72 shows the circuit around this 1.27 mm, 0° double row pin header (J5). The eight pins address the two different ICSP interfaces (Microchip Technologies Inc.) of both controllers. Therefore, the desired microcontroller is selected by selecting the appropriate programming cable. One cable, with the pins 1 (*VPP*), 3 (*PGD*), 5 (*PGC*), 7 (*VSS*) and 8 (*VDD*) used, addresses the dsPIC33EP128GM304 controller. The other cable uses the pins 2 (*VPP*), 4 (*ICSPDAT*), 6 (*ICSPCLK*), 7 (*VSS*) and 8 (*VDD*) for the PIC16F18325 semiconductor. To program the microcontrollers, an inexpensive programmer like the MPLAB PICkit 4 in-circuit debugger from Microchip Technology Inc. is needfully. As the name indicates, this programming tool can also be used for debugging and troubleshooting.

The programming pins of both controllers have two functions (Table 10, Table 11 and Table 12). In normal operation mode, *ledG* and *ledR* control the two LEDs in Figure 72 and *Tex6* / *Tex7* are analog sensor signals for the PIC16F18325. If the external temperature measurement controller PIC16F18325 should be programmed, the components R120, R121, C108 and C109 (Figure 71) has to be removed (please refer ICSP specifications).

6.8 Printed Circuit Board

One of the most important components, which significantly influences the functionality of the developed circuit, is the printed circuit board itself. A clear and functional implementation of the circuit diagram is only possible through well-considered arrangement and connection of the individual electronic components and consideration of mechanical specifications (dimensions, slots, mounting holes etc.). Particularly in the case of switched-mode power supplies and inverters, due to the high switching frequencies and the steep current and voltage rises, it is important to ensure a good layout. Parasitic inductances between the power switches and the DC-link capacitance should be as low as possible, since self-induced voltages can occur due to commutation processes of the currents. These inductances can be kept small by short circuit paths and wide conductor tracks.

6.8.1 Board Layout

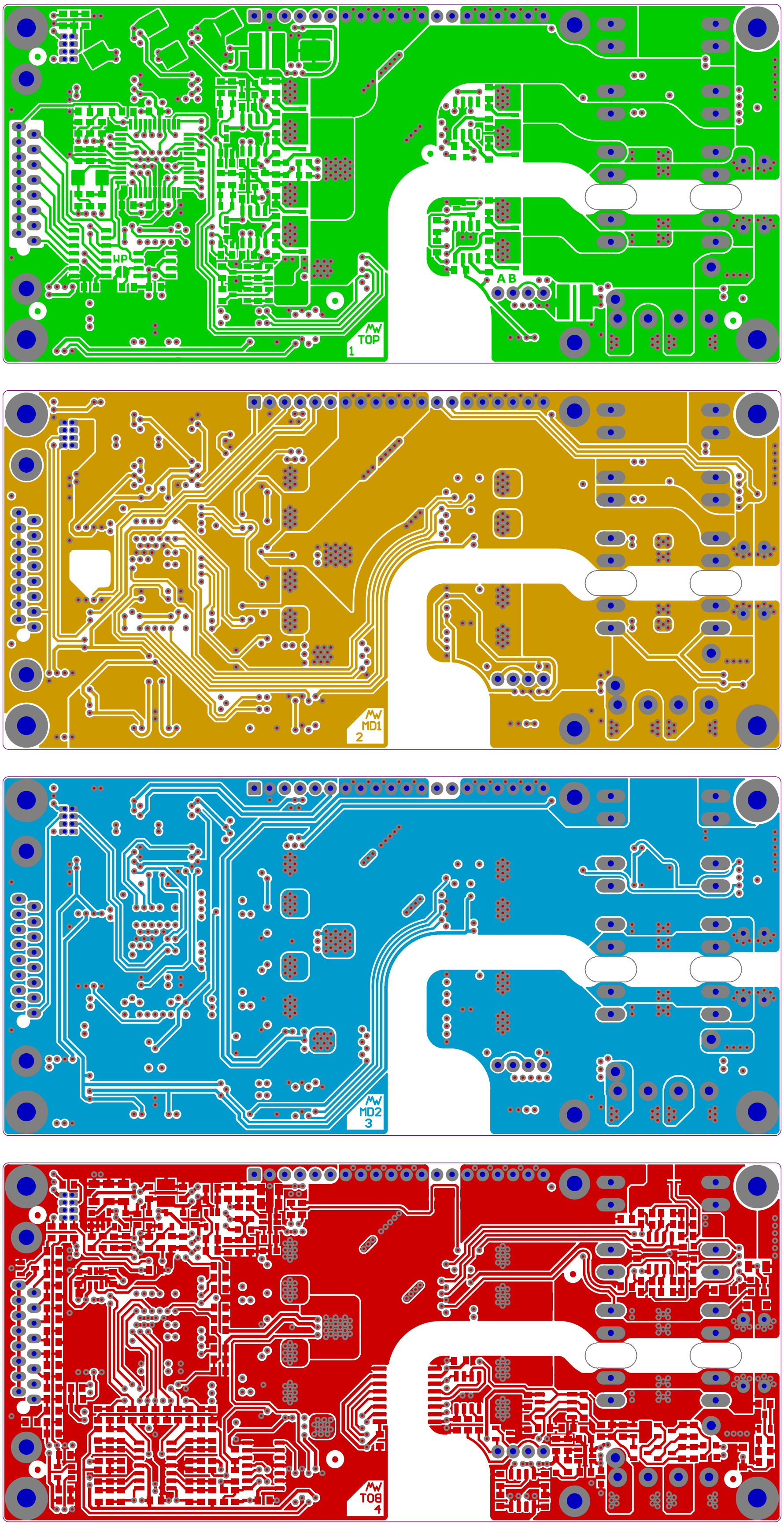
A printed circuit board made of FR-4 material with the dimensions 130×60 mm and a thickness of 1.6 mm is used to compactly combine all functions and components into one module. The prototype circuit board consists of four copper layers, each 70 µm thick. The layout for these four copper layers is shown in Figure 73 (top view) with each layer being assigned to a specific function/task as indicated in Table 13. The strict separation between the power and analog sections reduces interference and noise when measuring the accumulator cell voltage. In Figure 73 the potential separation between the primary and secondary side, which has been implemented on all copper layers, is also clearly visible.

Table 13 – Copper layers and their functions on the Platinfuchs IIa board

	layer	assigned function/task
1	TOP	power section with transformer, storage choke and power MOSFETs MOSFET driver circuits and auxiliary power sources (storage jokes) digital control unit with microcontrollers, memory and clock generation
2	MD1	power distribution and connections between the converter stages signal distribution and *ZVK*, *GND* and *3V3* areas for shielding
3	MD2	ground current (**GND** and *GND*) as well as signal distribution ground planes to shield the analog area from the converter stages
4	BOT	analog section with precision signal processing and measuring circuits precision voltage reference and analog signal distribution auxiliary power supplies and DC-link ceramic capacitors

Source: by the author

Figure 73 – Conductor paths on the TOP-, MD1-, MD2- and BOT-layers

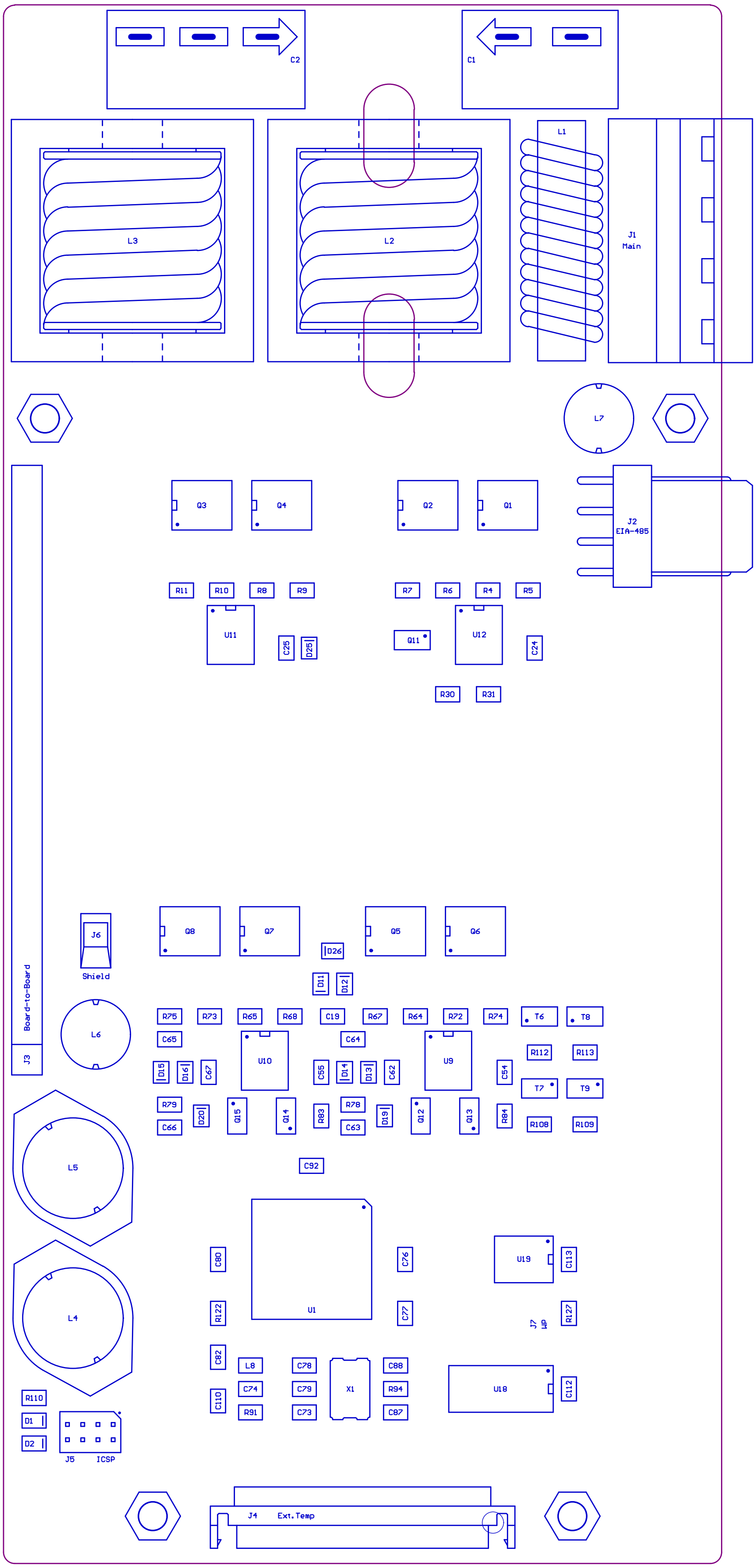


Source: by the author

6.8.2 Components Assembly Plan

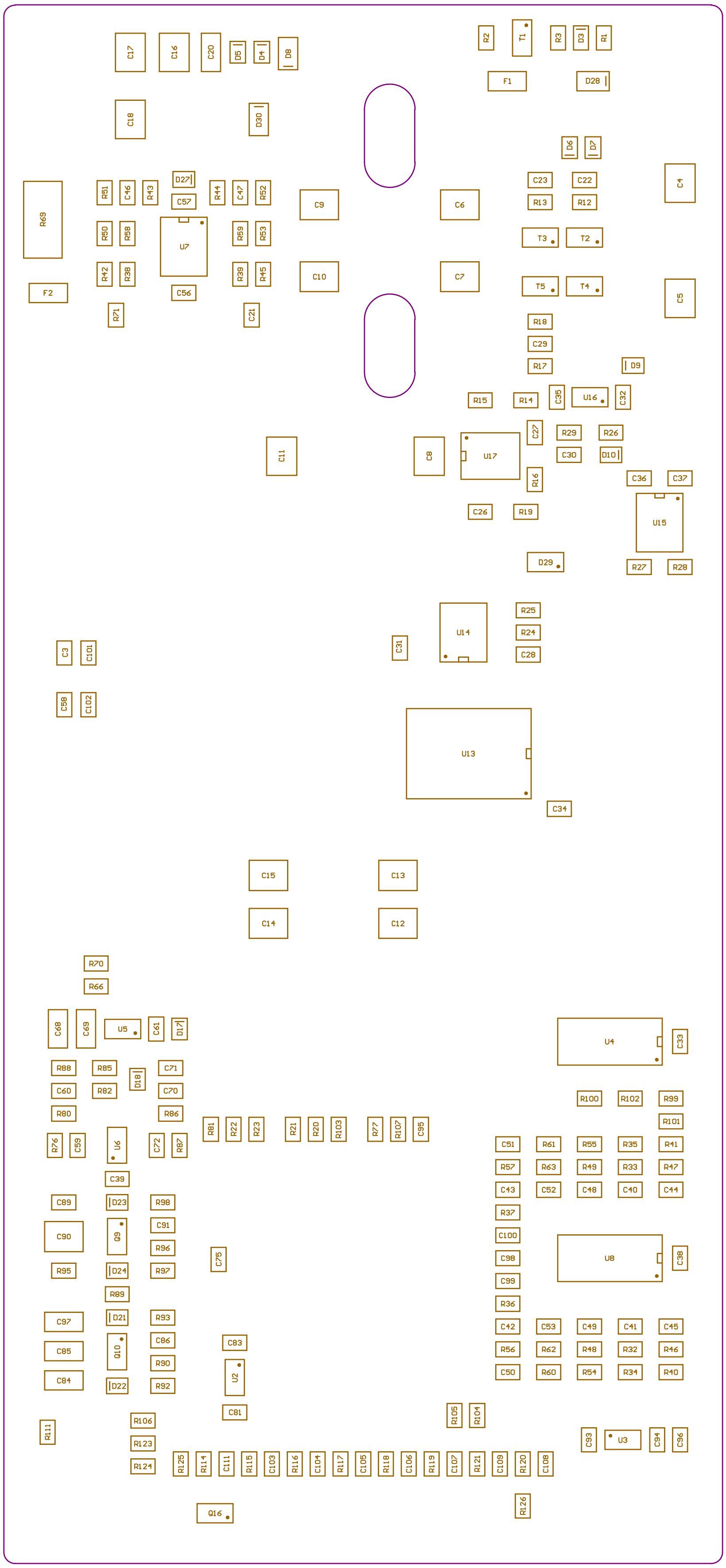
For reasons of space, the circuit board is equipped with the electronic components on both sides. The mounting position of each individual component can be seen in Figure 74 and Figure 75 (both top view). Due to the bulkiness and weight of the transformer, storage choke, filter inductance, electrolytic capacitors and all connectors, these components were attached using through-hole technology (THT). This enables an improved interconnection between the copper layers and a higher assembly strength than is possible with SMDs. The consistent use of surface-mound-devices (SMDs) for the power MOSFETs and their driver circuits as well as the digital control unit allows an area with a height of only 1.5 mm to be created in the center of the PCB (Figure 74). This enables the installation of a thermal gap filler and an 3 mm aluminum plate to dissipate respectively distribute the heat in this area (cooling of the power MOSFETs).

Figure 74 – Component position on the top



Source: by the author

Figure 75 – Component position on the bottom



Source: by the author

7 RESULTS

7.1 Step Response Analysis

The mathematical model can be checked using the real hardware of the Silberfuchs electronic. Ideally, a bode plot with magnitude and phase response is made for this purpose, whereby this should largely agree with the calculation. Unfortunately, creating a bode plot involves some extra effort, especially since the input signal must be available as a pulse-width modulation signal. Hence, a separate PWM generator is necessary to set the required α and β duty cycles ($\beta = 1 - \alpha$) over several frequency decades. This control signals must then be fed in at points *dcdc-Hi* and *dcdc-Lo*, and the PWM generation by the digital control system (microcontroller) must be deactivated.[1]

This effort can be avoided if the step response of the system is determined instead of the bode plot. Just like the bode plot, the step response describes the behavior of the system completely, since (ideally) all frequencies are available in the step. Thus, the transfer function for current and voltage of the battery management system can be verified by determining their step responses. An advantage is, that the step input signal for α (and β) can be generated simple by the digital control system that is implemented on the Platinfuchs IIa board. However, since the regulation is overridden, there is neither a voltage nor a current limitation. The set point value for α must therefore be chosen with care.

7.1.1 Voltage Step

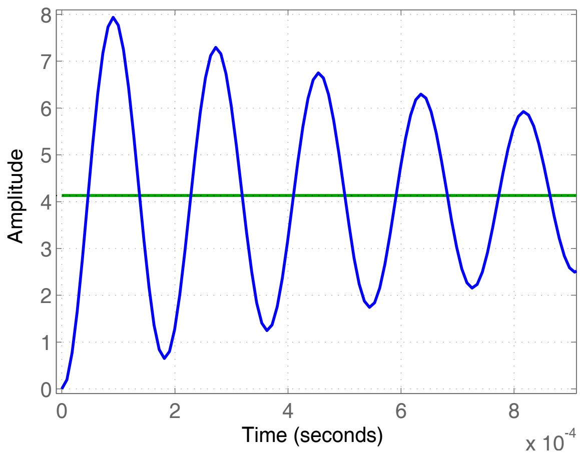
For the voltage step, the duty cycle α was set from 0 % to 50 % both in the simulation of the step response and in the hardware. Due to the undamped output, an overshoot occurs on the LC oscillating circuit, which tends to zero over time (Figure 76 and Figure 77). Apart from component deviations, the resonance frequency of the simulation is the same as that of the Platinfuchs IIa prototype board (please refer equation (59)). However, there is a difference in the decay of the oscillation. While the voltage at the hardware calms down within 800 µs (Figure 77), the simulation still shows a strong oscillation (Figure 76). It can be clearly seen that the damping of the LC resonant circuit (L3/C4 in Figure 34) is incorrectly represented by the state-space representation. This is because not all oscillating circuit losses were considered in the mathematical model. Copper resistances of the circuit board, ESRs of the ceramic capacitors and, finally, the loss of the ferrite material of the storage inductor (hysteresis and eddy current losses) are not included.[2]

---

[1] The controller has to continue to supply the push-pull converter with the γ and δ signals.
[2] These losses can only be determined more precisely with additional measurements.

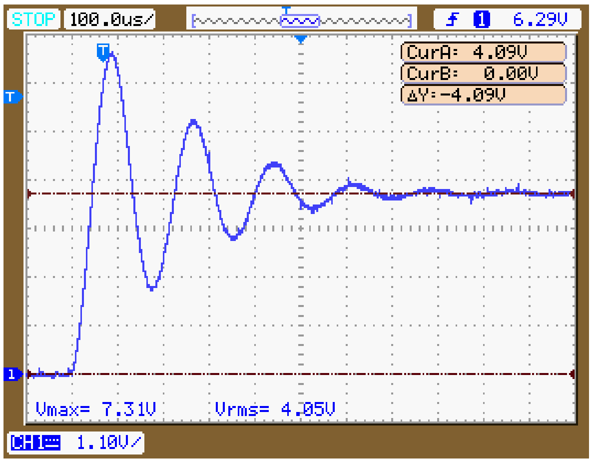
The PI input filter and the push-pull converter stage have a negligible effect on the voltage step response and apart from the different damping, the mathematical model created corresponds to the Platinfuchs IIa hardware. The voltage transfer function describes the system sufficiently and can therefore be used to model a voltage closed-loop control.

Figure 76 – Voltage step - Calculation



Source: by the author

Figure 77 – Voltage step - Hardware



Source: by the author

7.1.2 Current Step

In order to measure the step response of the current, the accumulator cell was replaced by a short circuit ($R = 0\,\Omega$). The output current I_{Out} was measured on the prototype using a $10\,\mathrm{m\Omega}$ shunt resistor, where this shunt was part of the output resistance R10 (Figure 31 and Figure 34).[3] Additionally, the duty cycle α was adjusted from $0\,\%$ to $7.85\,\%$ thanks to the microcontroller and also set in the mathematical model. This generates a current step of around 8.0 A for the simulation as well as for the Platinfuchs IIa prototype board (Figure 78 and Figure 79). The step response of the current has a time constant of approximately 150 µs both for the simulation and the hardware, which agrees well with the theory (equation (78)). The measured current of the hardware (Figure 79) does not reach the 8.0 A as the calculation dictates (Figure 78). The reason for this are the additional copper resistances of the circuit board, which were not considered in the mathematical model. In addition, interference from the switching operation of the DC/DC converter module can be seen on the 76 mV measurement signal in Figure 79.

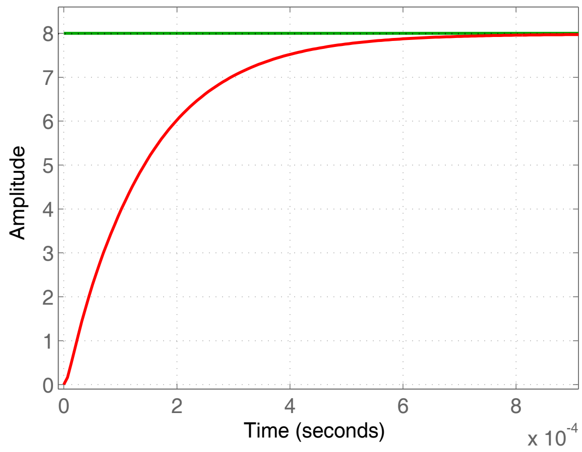
$$\tau_{Sync} = \frac{L_{L3}}{R_{R9} + R_{R10}} = \frac{12.2\,\mu\mathrm{H}}{9.53\,\mathrm{m\Omega} + 70.53\,\mathrm{m\Omega}} = 151.14\,\mu\mathrm{s} \tag{78}$$

As with the voltage step response, the behavior of the current step response is mainly determined by the synchronous converter. Inductance L3 and the total copper resistance in the output circuit determine the time constant τ_{Sync}. The PI input filter and the push-pull

[3] The total resistance of R10 was not changed.

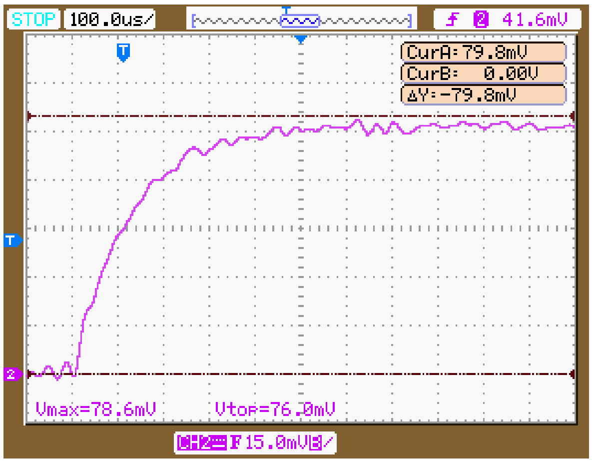
converter only have a minor influence on the current transmission function. As shown in Figure 78 and Figure 79, the mathematical model respectively transfer function matches the hardware and can now be used to model the current closed-loop control.

Figure 78 – Current step - Calculation



Source: by the author

Figure 79 – Current step - Hardware



Source: by the author

7.2 Cell Voltage Measurement Analysis

As already mentioned, the voltage is the most important indicator of an accumulator cell. The cell voltage not only has to be kept always within the voltage limits, its value also provides reliable information about the state of charge (SoC), state of health (SoH) and state of safety (SoS) of the cell. It is therefore important that the cell voltage measurement of each individual cell is carried out with high accuracy by the balancing electronic.

The Platinfuchs IIa prototype board uses an analog signal processing unit (analog front end), a microcontroller (U1) with an integrated 12-bit analog-to-digital converter (ADC) and a precise 0.1 % voltage reference (U2) to measure and digitize the cell voltage. Due to the limited accuracy of the integrated ADC (±5 LSB offset and ±10 LSB gain error) and the voltage reference, a one-time calibration of the offset and the amplification of the voltage measurement channel is necessary.[4] However, temporal fluctuations in the measurement signal cannot be corrected with the calibration. High-frequency electrical and magnetic interference generated by the DC/DC converters used are coupled into the measurement signals. The coupled-in noise respectively jitter is caused by signal crosstalk between the conductor paths of the printed circuit board (PCB) and can only be analyzed directly on the prototype electronic.[5]

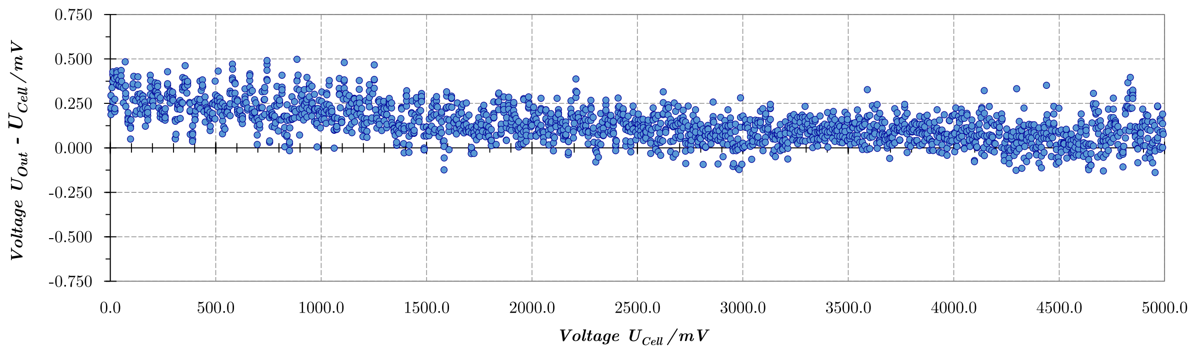
[4] Integral and differential nonlinearities (INL and DNL) of the ADC as well as the influence of a non-ideal common mode rejection of the AFE cannot be corrected with a simple adjustment.

[5] This ensures that the PCB with the arrangement of the components is also taken into account.

7.2.1 Influence of the Multiplexer Board

Since it is too expensive to provide a separate voltage measurement channel for each accumulator cell, the input of the analog front end (AFE) is switched directly to the desired cell thanks to the power multiplexer and the measurement is carried out. Since there is a multiplexer between the measuring system and the cell, the influence of this multiplexer on the measuring signal must be checked. Especially semiconductor relays, which are used for the multiplexer, deviate from the ideal switch and have undesirable switch-on resistances, leakage currents and charge injections. The bidirectional semiconductor switch specially developed for this battery management electronic has extra high charge injection, which can affect the measurement signal.[6] Therefore, Figure 80 shows the measurement of the deviation of the measured U_{Out} voltage and the cell voltage U_{Cell} depending on the full input range (0 V to 5 V) of the AFE. Each measuring point consists of 16 samples and was measured with the 16-bit NI USB-6210 multifunctional data acquisition system (NI-DAQ) from NI (formerly National Instruments) at zero output current ($I_{Cell} \approx 0$ mA). As can be seen in Figure 80, there is a voltage error of less than ±350 µV (with an offset of around 150 µV). For the cell voltage U_{Cell}, this measurement error of 0.07 ‰ from the full range can be ignored.

Figure 80 – Measurement deviation due to the multiplexer board



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7.2.2 Without Digital Filtering

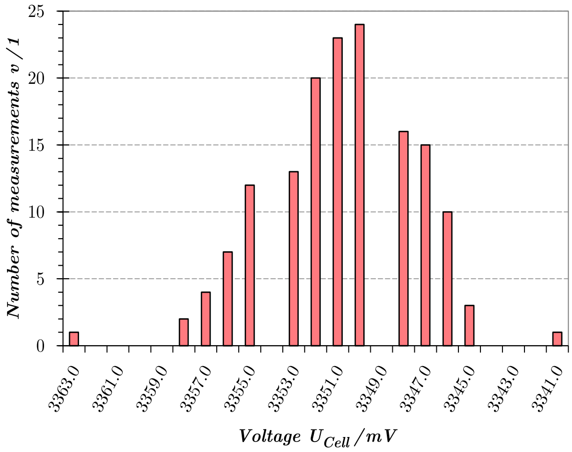
To determine the spread of the voltage measurement, an accumulator cell with a high capacity and a nominal voltage of 3.3 V was connected to the power multiplexer and numerous individual measurements were recorded directly with the balancer electronic. In addition, a Fluke 189 multimeter serves as a reference, as it shows the “true” voltage value of the cell.[7]

[6] The “Wenzistor” semiconductor switch topology allows extra low switch-on resistances and short switching times, but has peak currents of up to 1.2 mA for control.

[7] The Fluke multimeter was not calibrated and the deviation from the ideal value is unknown.

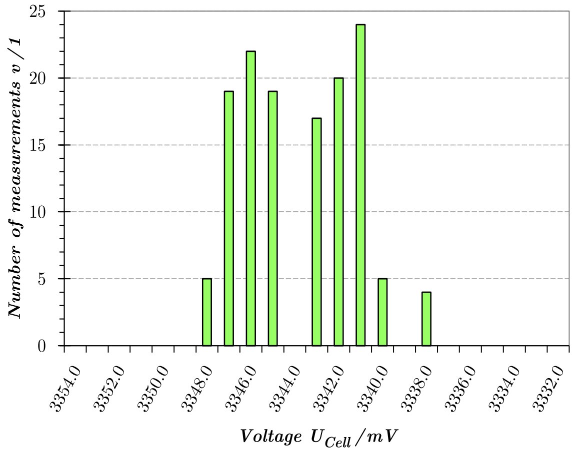
Figure 81 shows 151 individual measurements and their distribution within a 22 mV range. While the arithmetic mean of the measured values is 3351.5 mV, the Fluke multimeter shows 3357.7 mV. The individual measured values vary from the mean value by up to ±6.5 mV, whereby two measured values (3363.0 mV and 3341.0) are still far outside this range. Therefore, in the worst case, the deviation can be assumed to be ±11.5 mV. The behavior improves if the full-bridge circuit (synchronous converter) is disabled, as it is necessary for a cell voltage measurement. Figure 82 presents 135 measured values when the converter is deactivated. The mean value is 3343.8 mV (Fluke: 3350.3 mV) with a deviation of maximum ±5.8 mV.[8]

Figure 81 – One sample measured; full-bridge enabled



Source: by the author

Figure 82 – One sample measured; full-bridge disabled

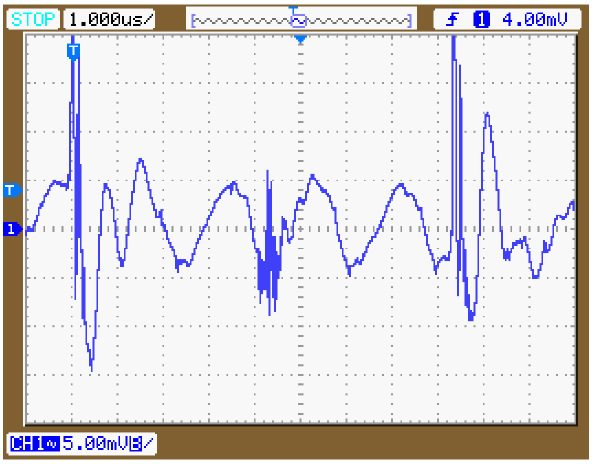


Source: by the author

The deviation of ±5.8 mV (disabled full-bridge) is good enough for an over- and under-voltage detection. However, the accuracy is too low to draw conclusions about the state of charge (SoC) of the accumulator cell, especially for $LiFePO_4$ cells. A cause analysis with an oscilloscope showed that the jitter of the voltage measurement is mainly due to a suboptimal layout. Figure 83 and Figure 84 present a voltage offset between the reference ground of the ADC and the ground of the output filter (R37/C43 and R57/C51 in chapter 6) of the analog front end. Both points there are aGND potential and should have the same voltage, but the small distance of approximately 25 mm on the printed circuit board is sufficient for electromagnetic interference to change the voltage. Disabling the synchronous converter reduces the problem, but a large part of the disturbance remains. As can be seen in Figure 84 this disturbance fluctuates with approx. 500 kHz which fits well with the switching frequency of the 3.3 V auxiliary supply (U5 in Figure 60). This frequency is high enough to be removed using a low-pass filter.

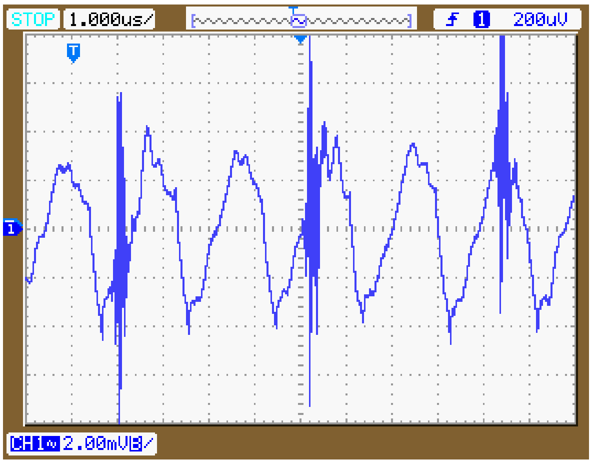
[8] The gaps between the bars in Figure 81 and Figure 82 are caused by rounding errors in the microcontroller when converting binary data into decimal representation.

Figure 83 – Measured voltage jitter; full-bridge enabled



Source: by the author

Figure 84 – Measured voltage jitter; full-bridge disabled



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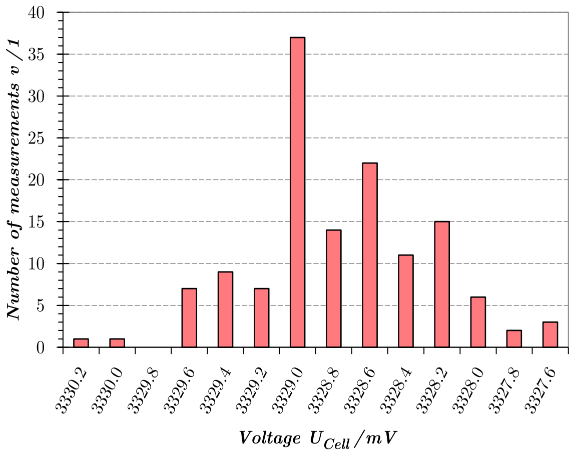
7.2.3 With Digital Filtering

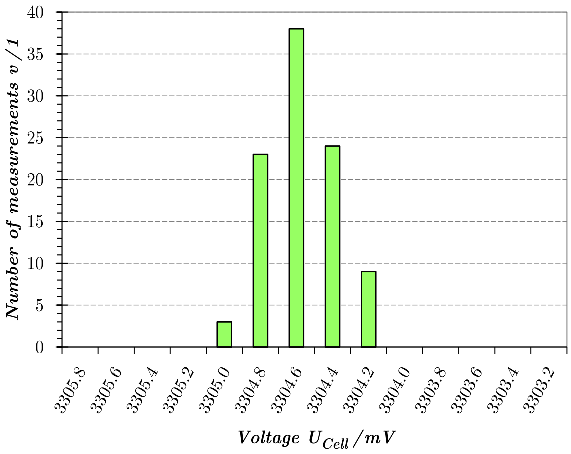
To reduce the jitter and noise on the measured voltage signal, a simple digital filter was implemented with the help of an algorithm. For this reason, the cell voltage is measured continuously and after 32 samples an arithmetic mean value is calculated. This oversampling increases the measurement time by a factor of 32, but the result is a significantly better resolution of the cell voltage signal. Ideally, 14.5 bits are available for digitizing the analog signal (with the sign 15.5 bits).[9] Unfortunately, the real achievable resolution still depends on the noise and jitter of the input signal. As before, the voltage measurement must therefore be validated using a high-capacity accumulator cell and the Fluke 189 multimeter.

Figure 85 – Average of 32 samples; full-bridge enabled



Source: by the author

Figure 86 – Average of 32 samples; full-bridge disabled



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[9] An oversampling of factor 32 creates an additional 2.5 bits.

Figure 85 and Figure 86 present the measured voltage values, with each individual measurement consisting of 32 samples. In Figure 85, 135 measured values are distributed over a range of 2.60 mV (full-bridge respectively synchronous converter enabled). These values only deviate from the arithmetic mean (3328.8 mV) by a maximum of ±1.40 mV (Fluke measured value: 3330.3 mV). The noise can be further reduced by deactivating the full-bridge circuit, as it is necessary for a cell voltage measurement (Figure 86). The measured voltage for 97 measures now only fluctuates ±500 µV around the mean value of 3304.7 mV (Fluke: 3309.5 mV). Compared to measurements without a filter, this is better by a factor of around 11 and enables the state of charge (SoC) of an accumulator cell and its change over time to be reliably determined.

7.3 Power Conversion Analysis

To evaluate and prove the performance of the power stages of the Silberfuchs balancer electronic, the currents and voltages at the input and the output were recorded if changing load conditions. In addition, the voltage and current between the Platinfuchs IIa and the Polarfuchs IIa boards at connection *Line1* and *Line2* were also measured. To minimize the influence on the measurements, a low-inductance 1 mΩ shunt resistor was inserted at point *Line1* to meter the current. All measured voltage and currents were recorded with special designed analog isolation amplifiers, which were adapted to the metering task in terms of amplification and bandwidth. The fine adjustment of offset and gain was carried out on all isolation amplifiers using two 10-turn potentiometers directly on the amplifier. For this purpose, a Fluke 189 multimeter was used as the reference device. Although the multimeter was not calibrated, relative measurements, as required for efficiency, can be carried out with high accuracy (around ±0.10 %). In the case of an absolute measurement (power loss) an error of approximately 0.50 % must be expected.

The prepared analog measured values were digitized with the NI USB-6210 data acquisition system (NI-DAQ) and transferred to a computer system for analysis. The values were processed with a LabVIEW program (also from NI). Thereby, the signals were filtered (averaged), input, intermediate and output power were calculated, efficiency and losses were determined, and all values were saved for further processing. In addition, the LabVIEW program was also used to visualize and check the plausibility of all values.

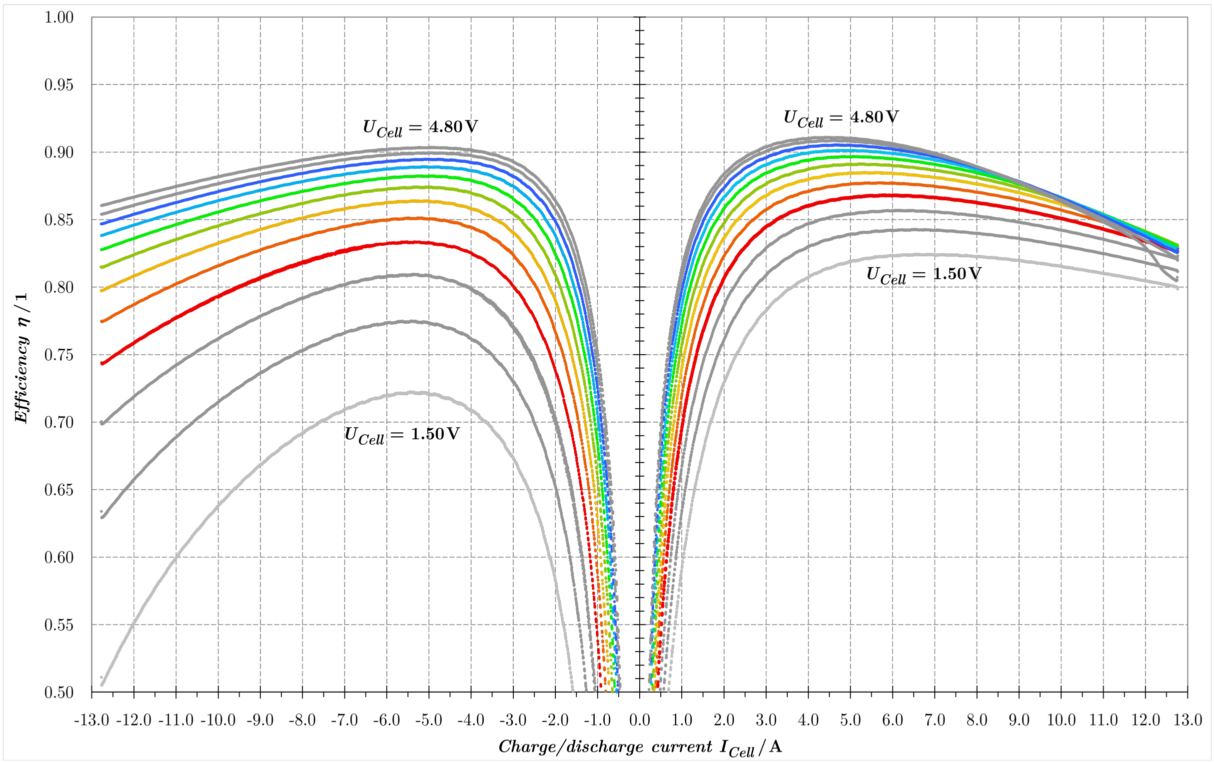
7.3.1 Efficiency

To get an efficiency curve, 30 values were measured per second, with each measuring point consisting of 1000 samples (average). Each measurement curve was recorded over a period of around 200 s, which led to approximately 6000 measurement points per curve.

During each measurement, the cell current I_{Cell} was continuously increased from zero to 12.80 A (charge mode) thanks to a controlled constant current source/sink circuit (for discharge mode: −12.80 A). In addition, the cell voltage U_{Cell} was regulated to a constant value by the balancing electronic.[10] To obtain a set of curves, the cell voltage (setpoint voltage) was changed in 300 mV steps, starting with 1.50 V and ending with 4.80 V.

Figure 87 shows the efficiency both for discharge operation (left side) and for charge operation (right side) of the DC/DC converter board Platinfuchs IIa.[11] Although the energy conversion takes place via two converter stages (push-pull and synchronous converter) and extensive peripheral units are supplied, a peak efficiency of 91.10 % at 4.80 V can be achieved. At a typical lithium-ion cell voltage of 3.60 V (light green curve), an efficiency of up to 89.50 % for charging and 88.20 % for discharging is reachable (in each case at 5.00 A charging respectively discharging current).

Figure 87 – Efficiency of DC/DC converter board Platinfuchs IIa



Source: by the author

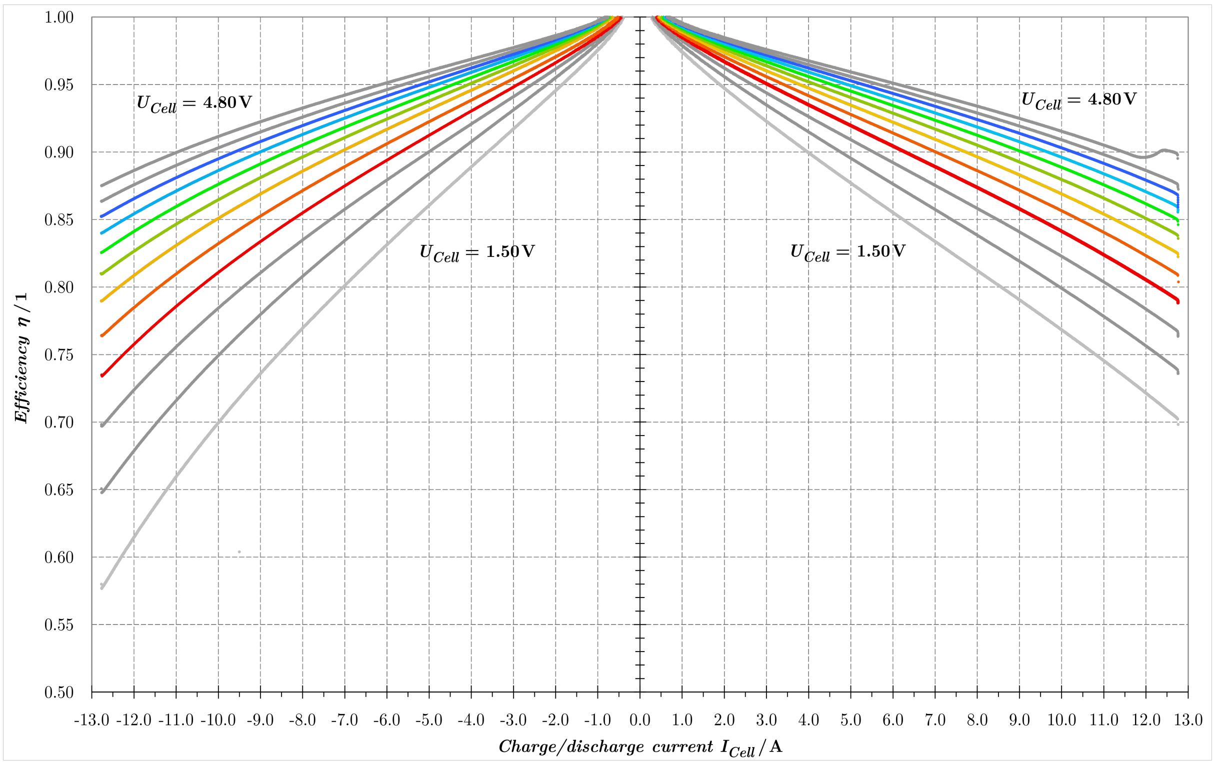
The efficiency of the multiplexer board Polarfuchs IIa is shown in Figure 88 and is in a wide range over 80.00 % both during charging and discharging. Since the power supply for the control system (microcontroller) and for the bidirectional power switches of the multiplexer are implemented on the DC/DC converter board, the efficiency of the

[10] For this purpose, the internal voltage feedback for the closed-loop control was shifted from the points *Line1* and *Line2* directly to the output of the balancer.

[11] The non-linearity of the curve at high charging currents (> 11.0 A) comes from saturation of the voltage measuring amplifier used.

multiplexer circuit depends purely on the ohmic losses of the power switches, the printed circuit board and the input and output connectors.[12]

Figure 88 – Efficiency of power multiplexer board Polarfuchs IIa



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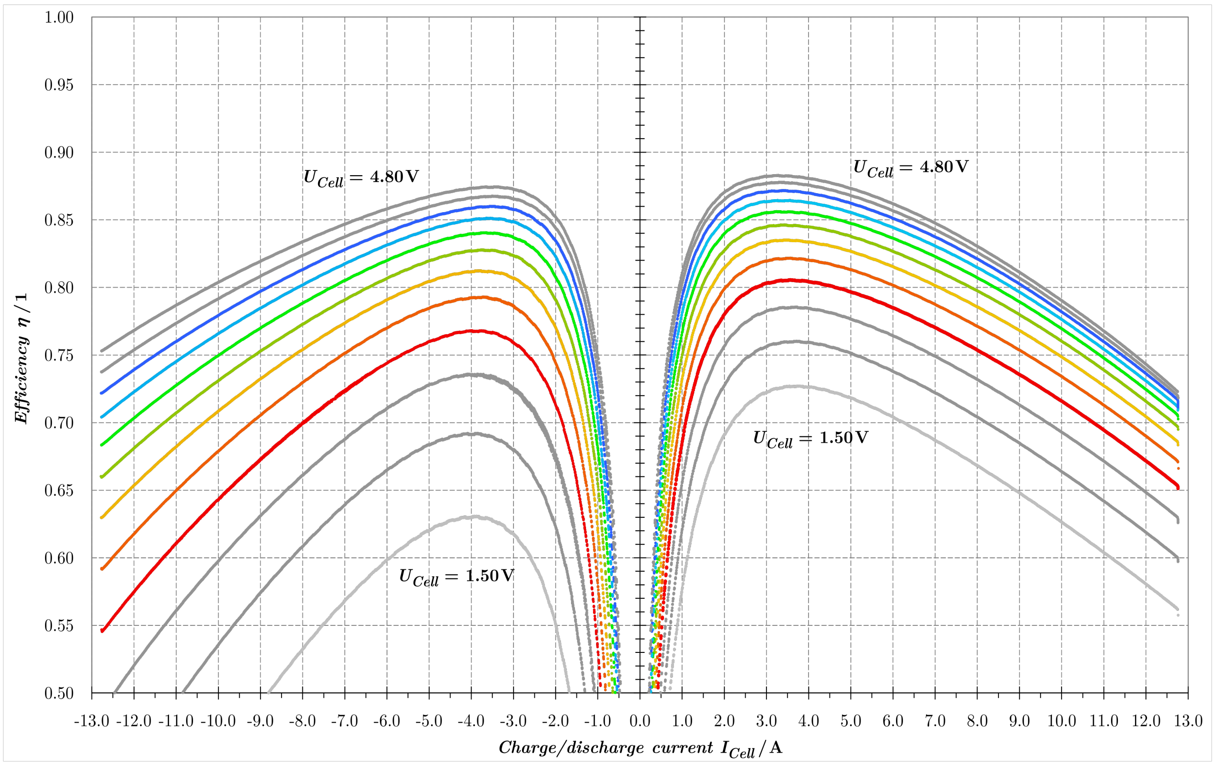
The overall efficiency is further reduced due to the series connection of the DC/DC converter and the power multiplexer. This efficiency is presented in Figure 89 for a cell voltage of 1.50 V to 4.80 V. From the set of curves, it is easy to see that the optimal current for balancing an accumulator cell is between 2.50 A and 5.50 A, as this is where the efficiency is highest for each cell voltage. Regardless of this, the balancing electronic allows supporting the selected accumulator cell with peak currents up to 12.80 A. Thereby, the efficiency is reduced to an average of around 70.00 %.

The typical operating range of the Silberfuchs balancing electronic depends on the type of accumulator used (Table 1). It can be assumed that the voltage of the accumulator cell will be in the range of 2.40 V to 4.20 V (red and blue curve in Figure 90). Furthermore, the continuous current must be limited to ±10.00 A due to the high thermal losses of the balancer. Thereby, the recommended operating range for the Silberfuchs balancer can be seen in Figure 90.

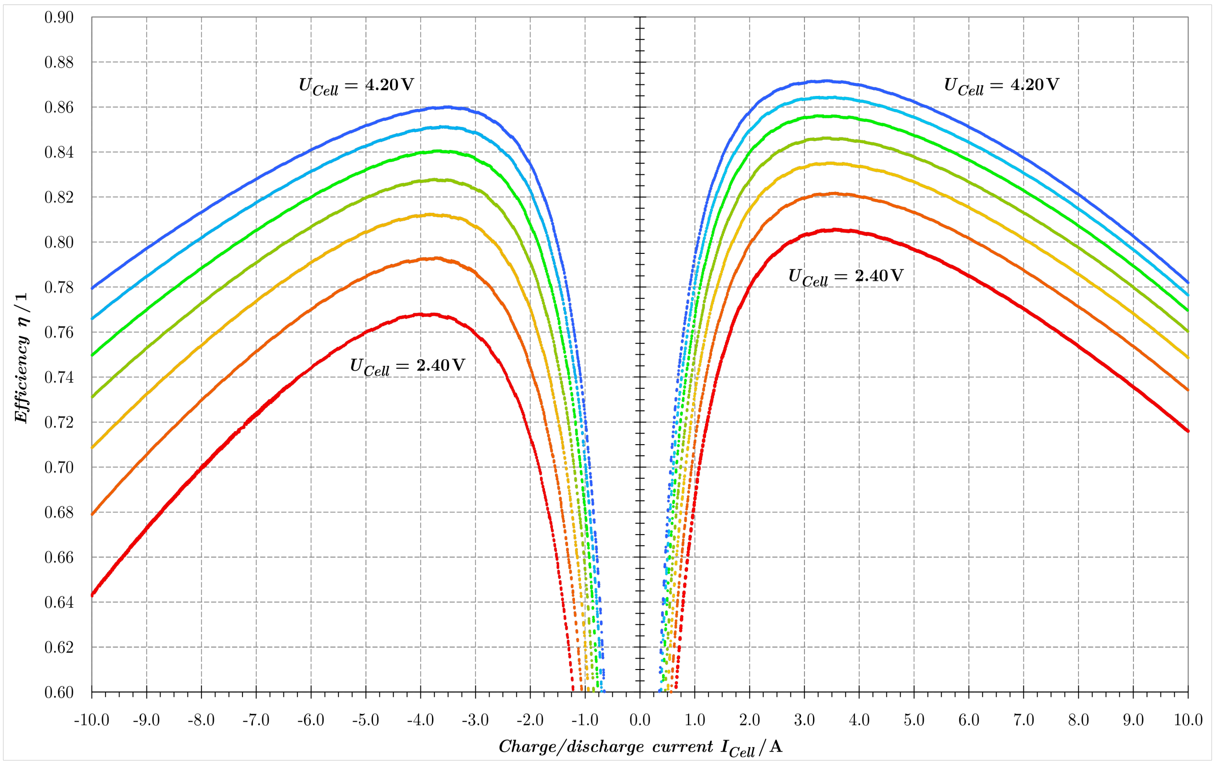
[12] The power that the multiplexer takes from the *3V0* and *VDD* supplies has already considered account in Figure 87.

Figure 89 – Efficiency of the total electronic (Silberfuchs balancer)



Source: by the author

Figure 90 – Efficiency of the total electronic - ±10.0 A range

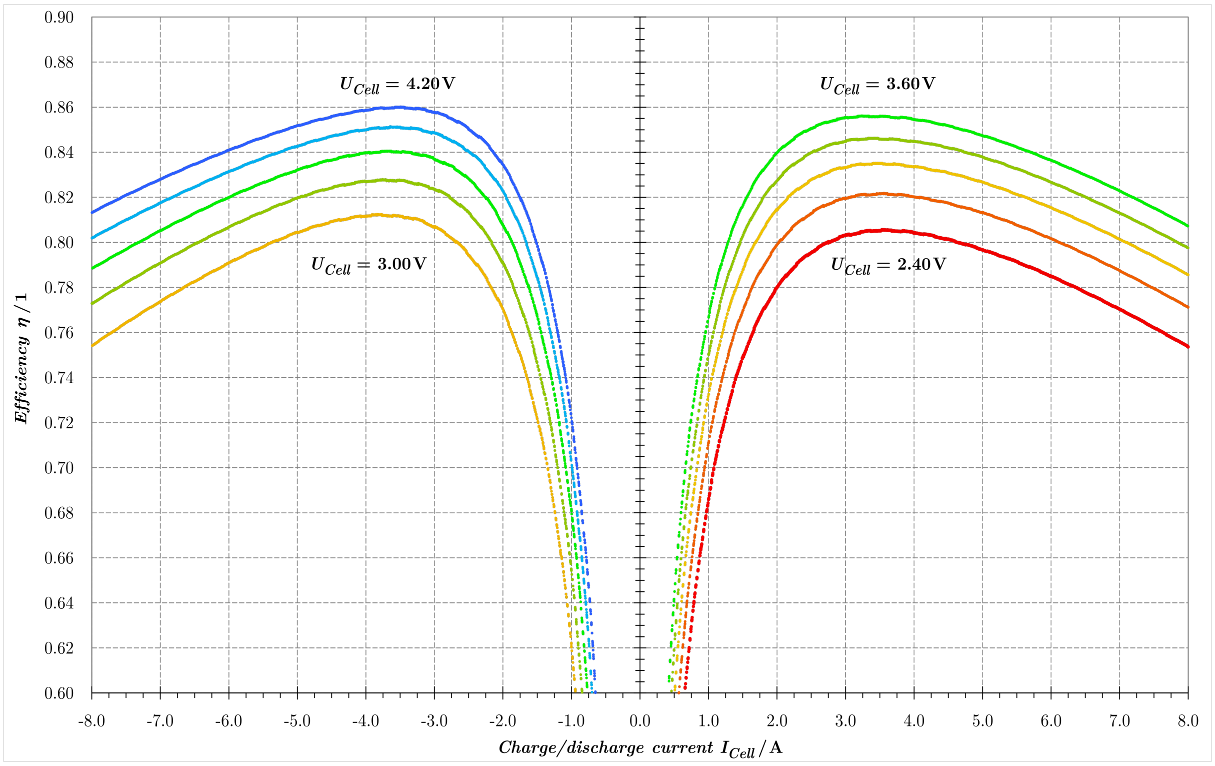


Source: by the author

Since the accumulator cell is typically charged at low cell voltage and is discharged when the cell voltage is too high, the working range of Figure 90 can be further restricted.

This restriction leads to the set of curves of Figure 91. In addition, the current range in the figure was restricted to 8.00 A. This optimization further reduces the thermal losses, but still allows the cell to be balanced within a short time. Thereby, the efficiency is over 75.00 % over the entire range. At the optimal working point of around ±4.00 A, the Silberfuchs battery management system achieves an efficiency between 80.50 % and 86.00 %.

Figure 91 – Efficiency of the total electronic - ±8.0 A range



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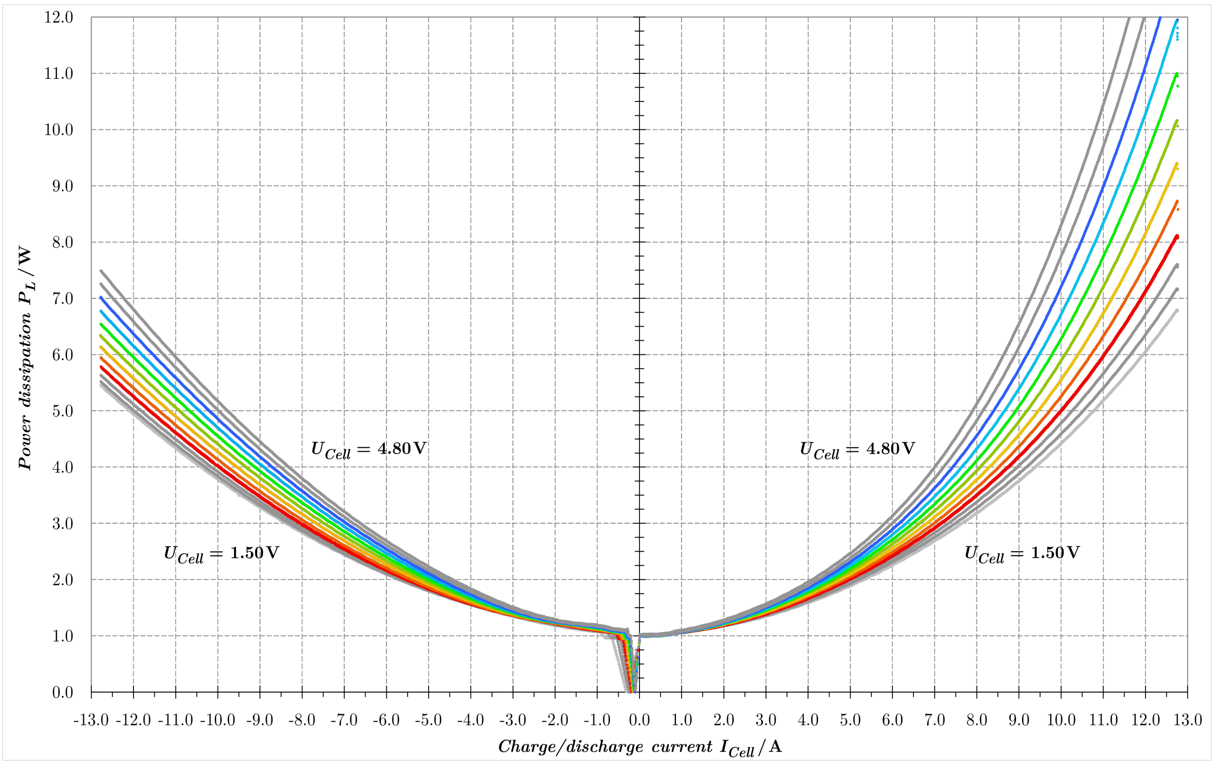
7.3.2 Power losses

The performance and lifespan of the Silberfuchs balancer circuit depend largely on the temperature of the electronic. The temperature is mainly dependent on the power loss generated and the heat transfer to the environment. Since neither a heat sink nor a fan is provided, the heat can only be transferred from the printed circuit boards to the ambient air by convection. Therefore, the losses of the individual boards should be as low as possible, which requires a high degree of efficiency.

The measurement data for current and voltage used for the efficiency calculation also enable the direct display of the heat losses. The measuring points, each consisting of 1000 individual samples, can be displayed over a charge/discharge current range of ±12.80 A. Equal to the efficiency diagram, a single curve consists of approximately 6000 measuring points.

Figure 92 shows the power dissipation of the DC/DC converter board Platinfuchs IIa for all cell voltages from 1.50 V to 4.80 V (300 mV steps).[13] The power loss increases in a parabolic manner and reaches the highest value with 16.30 W (not in the diagram) at 12.80 A. The standby power, at which all peripheral electronic circuits work, but no energy is transferred to the accumulator cell ($I_{Cell} = 0.0$ A), is around 1.00 W.

Figure 92 – Power loss of DC/DC converter board Platinfuchs IIa



Source: by the author

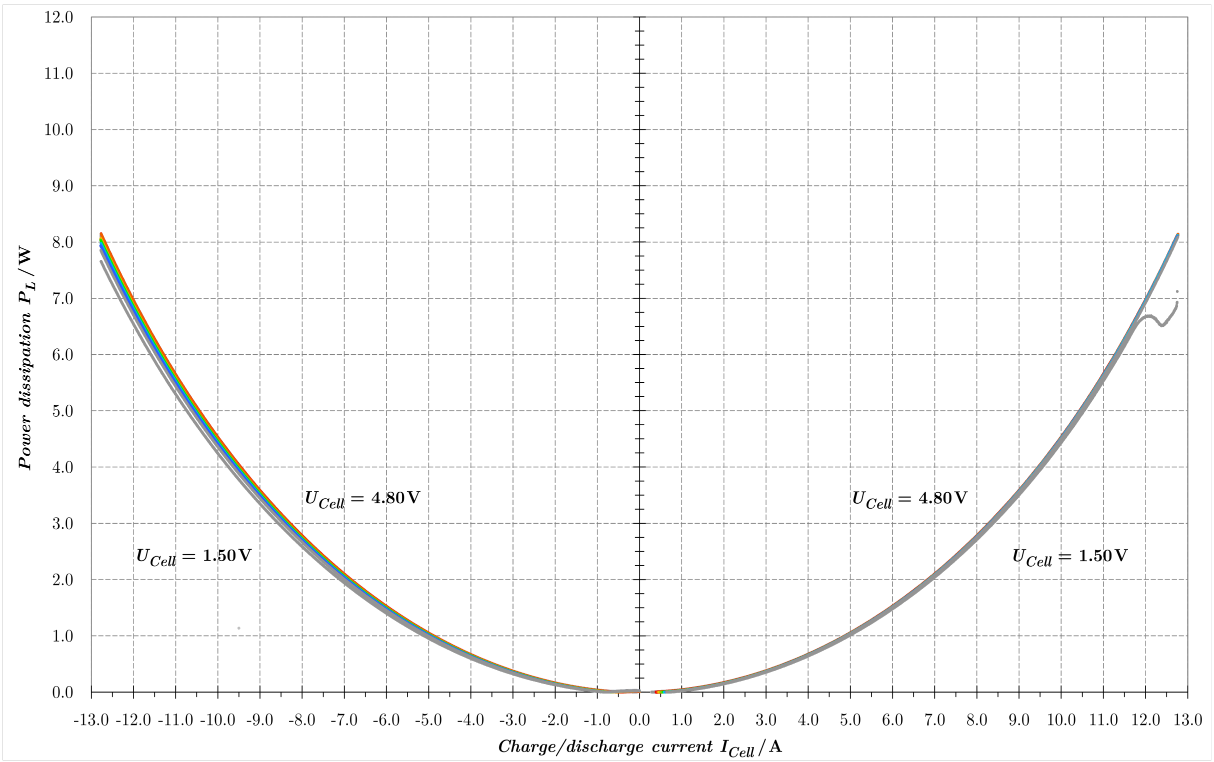
The power dissipation of the multiplexer board Polarfuchs IIa, shown in Figure 93, depends solely on the switch-on resistance of the two activated power switches and the ohmic resistance of the connectors and the conductor path of the PCB.[14] The symmetrical parabolic rise in Figure 93 can be reconciled with the equation $P_L = I_{Cell}^2 \cdot R$ and results in a substitute resistance for the two switches of around 22.5 mΩ each (in total 50 mΩ).

The total power loss of the Silberfuchs balancer (Platinfuchs IIa plus Polarfuchs IIa board) is presented in Figure 94. The charging and discharging losses differ substantial, as different powers are transmitted at the same current. For example, when discharging with 10.00 A at a cell voltage of 3.30 V, a power of 33.00 W is consumed, whereas in charging mode, 10.40 W of power losses must be added to the cell charging power of 33.00 W (in total the charging mode consumes 43.40 W).

[13] Those power losses in the figures that approach zero (curve peak between 0 A and −0.5 A) are incorrect. The absolute value of input and output power have been subtracted from each other ($P_L = |P_1| - |P_2|$), but in this range the circuit draws energy from both sides, which leads to a calculation error. The approximated power loss in this area is always around 1.0 W.

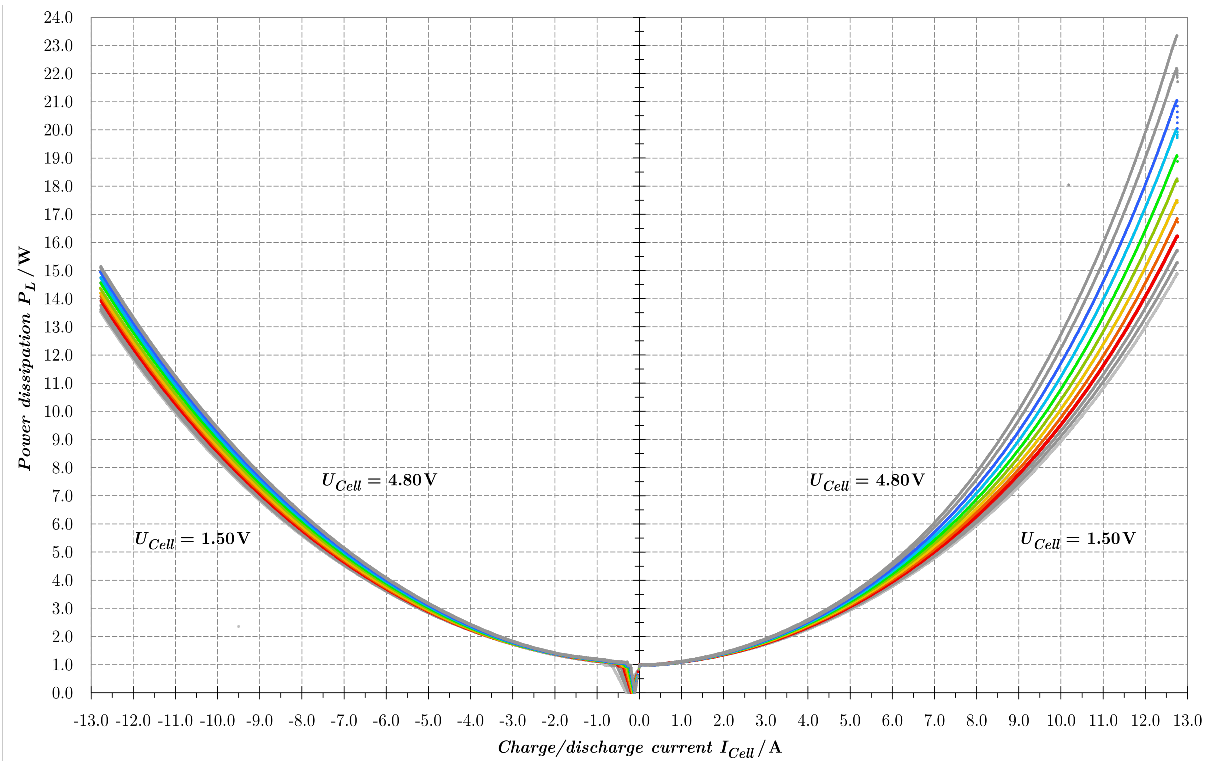
[14] The supply for the control unit and the power switches are included in the DC/DC converter board.

Figure 93 – Power loss of power multiplexer board Polarfuchs IIa



Source: by the author

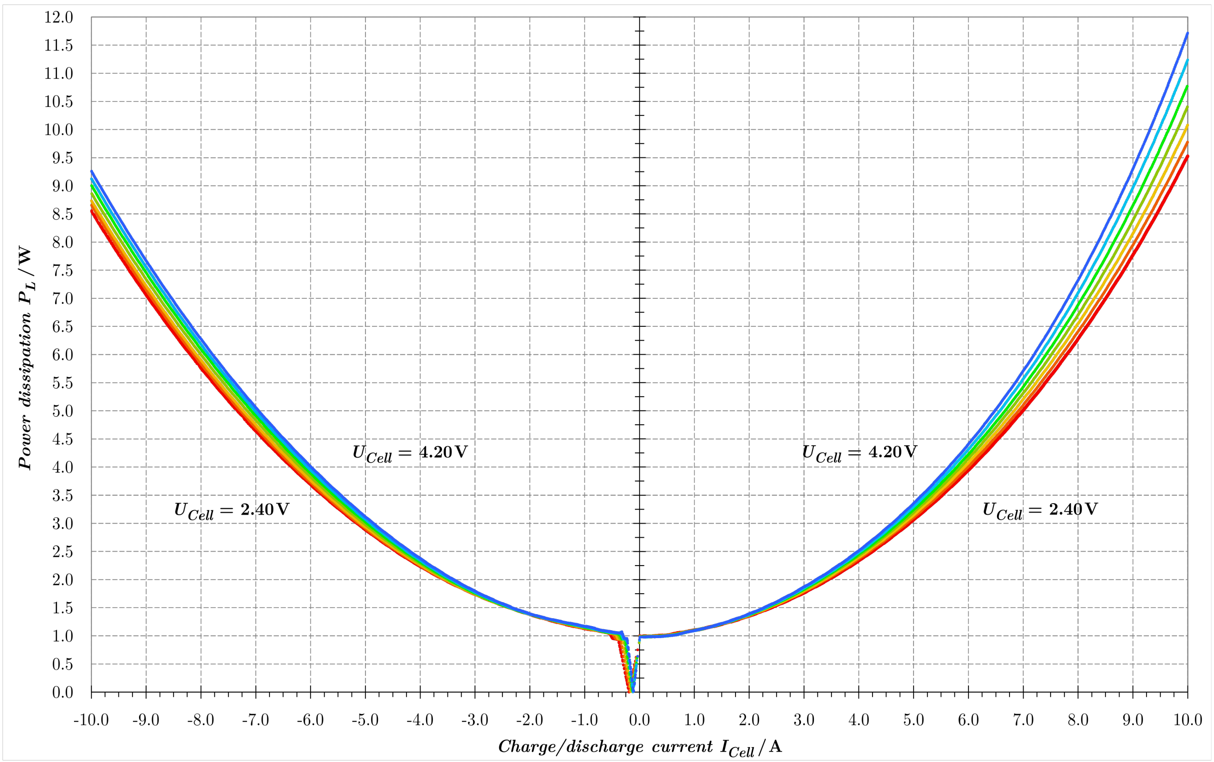
Figure 94 – Power loss of the total electronic (Silberfuchs balancer)



Source: by the author

The peak power loss of 23.30 W in Figure 94 is too high for a continuous operation. The accumulator cell can only be supported briefly with high currents. For a continuous operation, the charging and discharging currents must be limited to 10.00 A. This reduces the power dissipation to less than 12.00 W (Figure 95). In Figure 95 also, only the curves for the important voltage range of the accumulator cell from 2.40 V to 4.20 V is presented. Regardless of the real losses, the cell should be charged or discharged with 2.50 A to 5.50 A, since the energy is best used in this operating range (highest efficiency).

Figure 95 – Power loss of the total electronic - ±10.0 A range



Source: by the author

7.3.3 Simulation Comparison

The mathematical model from chapter 5 can also be used to determine the degree of efficiency, respectively losses. For this, the state-space representation in equilibrium, where all derivatives become zero, is used (equation 79). In this case, there is no voltage drop across the inductances L1, L2, L3 and L4 as well as no current flows across the capacitors C1, C2 C3 and C4. In a state of equilibrium, the internal currents and voltages depend solely on the individual resistances in the circuit. Since not all resistances are exactly known or have been considered (conductor tracks on the PCB), the model will deviate from reality.

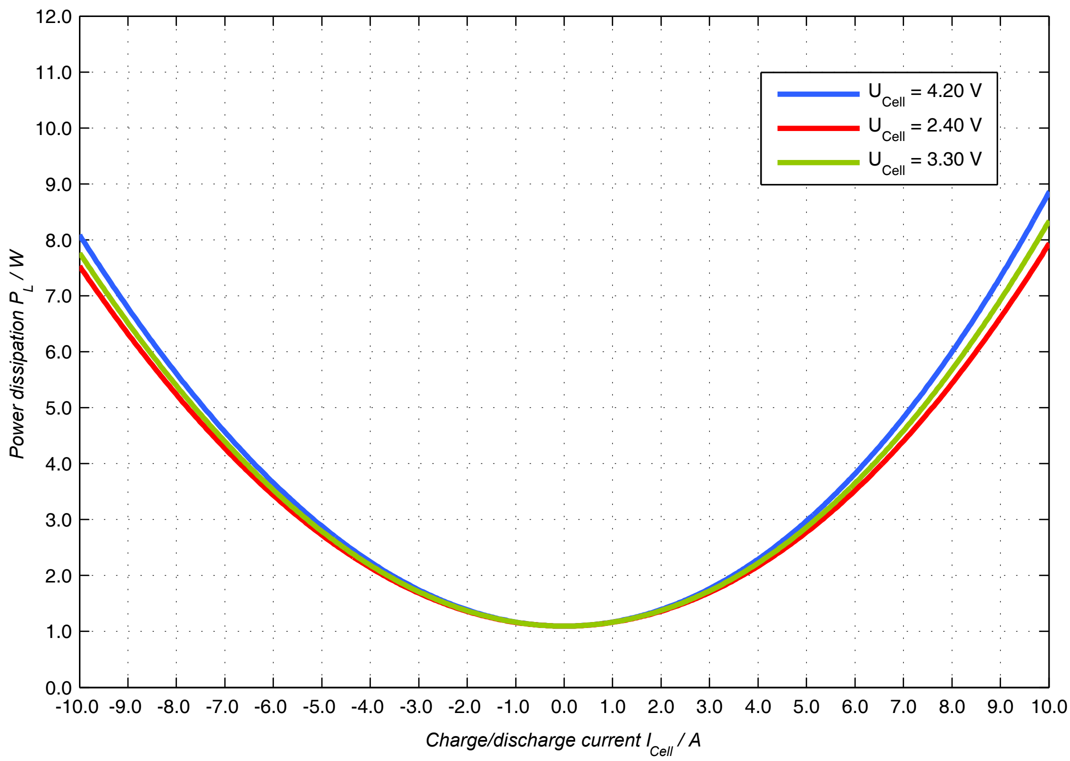
$$\mathbf{0} = \mathbf{A} \cdot \mathbf{X} + \mathbf{B} \cdot \mathbf{U} \tag{79}$$

In order to compare the power loss of Figure 95 with the simulation, some modifications in the state-space representation of equation 50 are necessary. Since the input and output power was measured directly at the connector of the DC/DC converter and the power multiplexer board, the resistance of the connection cables (cooper cable from the 12 V main supply and the balancing cable to the accumulator cell) must be eliminated in the mathematical model. This means that the resistance R_{R1} has to be changed from 46.78 mΩ to 0 mΩ and R_{R10} changes from 70.53 mΩ to 52.99 mΩ. Then equation 79 can be used to calculate the individual currents and voltages of the replacement circuit. The power loss of the entire electronic can be calculated using the equation 80. Whereby U_{U1} is the voltage of the 12 V main supply, U_{U2} is the voltage of the accumulator cell and I_{L4} corresponds to the charge/discharge current of the cell (I_{Cell} respectively I_{Out}).

$$P_V = U_{U1} \cdot I_{L1} - U_{U2} \cdot I_{L4} \tag{80}$$

The calculated power dissipation can be shown as a set of trajectories in a diagram. The Figure 96 shows the power losses for three different cell voltages. While the 2.4 V (red curve) and the 4.2 V (blue curve) graphs show the minimum and maximum range of a cell voltage, the 3.3 V curve (green) represents the typical cell voltage of a $LiFePO_4$ accumulator cell. The diagram was scaled in the same way as figure Figure 95. This allows a simple comparison between the realized prototype hardware and the mathematical model.

Figure 96 – Power loss of the total electronic - mathematical model



Source: by the author

The standby losses, when the accumulator cell is neither charged nor discharged ($I_{Cell} = 0.0$ A), for the mathematical model is 1095 mW. Regarding the prototype electronic.

only around 1000 mW was measured. The +9.5 % difference can be attributed to the iron loss of the transformer. This ferrite core loss was determined for the simulation using the data sheet, whereby the influence of the operating temperature and the actual flux density is difficult to consider.

The simulation of the total losses shows a deviation of approximately −12.5 % from reality at I_{Cell} is −10.0 A (green curve on the left side of Figure 96). As noted in the step response analysis, not all losses have been taken into account in the mathematical model. For example, the copper losses of the circuit board, dead time and switching losses of the power MOSFETs are unknown. In addition, there are parameter deviations of the power semiconductors from the values given in the data sheet (tolerances from R_{DSon}).

The deviation between the mathematical model and prototype electronic reaches a maximum at +10.0 A. While the simulation is too low by −15.8 % for a cell voltage of 2.40 V, this error increases to −18.4 % for 3.30 V and to −23.9 % for 4.20 V. This significant deviation from reality is largely due to the heating of the electronic. The R_{DSon} of the power MOSFETs increases by about 0.47 %/K and the resistance of the copper windings of the transformer and the storage inductance increases by 0.39 %/K, which means that at an operating temperature of 60 °C, the resistance is approximately 15 % higher and accordingly generates higher losses.[15]

Since, as stated, neither temperature effects, deviating component parameters nor all loss resistances (conductor tracks) were considered in the mathematical model, this model deviates from reality. Large errors are to be expected, especially in the case of small transferred power, as in this case. However, the mathematical modelling can be used as a first approximation and to optimize the electronic circuit. To consider all influencing factors, including the temperature, a prototype set-up of the electronic is recommended.

[15] The same applies to the individual "Wenzistor" semiconductor switches at the power multiplexer board.

8 CONCLUSION

Every modern chemical energy storage system, consisting of several accumulator cells connected in series, requires a well-optimized monitoring and balancing electronic. An active battery management system, as described in this work, allows the storage capacity and the existing charge of the battery stack to be used in the best possible way. A premature switch-off due to already weakened (aged) accumulator cells can be delayed by the energy redistribution within the battery stack. This leads to a significantly longer operating time (around 15 %, depending on the age of the cells). In addition, the service life of the energy storage system is extended because the individual accumulator cells are less stressed. This saves maintenance and manufacturing costs and relieves the burden on the environment, since the battery does not have to be replaced until later.

The presented battery management system Silberfuchs with a balancing power of up to 45 W allows high-capacity battery systems like those used in home batteries, large battery storage power stations and electrical vehicles to be balanced in a short time. The particularly high balancing current of up to ± 10 A enables a "weak" or pre-damaged cell to be actively supported. Whereby part of the energy is no longer supplied by the cell but by the balancing electronic. This increases the lifespan of the ailing cell and consequently the entire battery significantly. This advantage, which should not be underestimated, is made possible by the high efficiency of the active balancing electronic. Charging and discharging of an accumulator cell at the optimum operating-point can be done with an efficiency between 80 % and 85 %, as it is shown in this work. The high level of efficiency allows the entire electronic of the Silberfuchs active battery management system to be accommodated in a compact $130 \times 63 \times 18$ mm unit, which makes it interesting, for example, for electric vehicles. Furthermore, the measurement of the individual cell voltages with a resolution in the millivolt range enables the state of charge (SoC) to be determined precisely. The additionally integrated temperature measurement allows conclusions to be drawn about the state of health (SoH) and state of safety (SoS). In addition, thanks to active measurement methods (e.g., electrochemical impedance spectroscopy), an analysis of the electrochemical processes and changes within the cell is also possible. These extra functions can be added elegantly by adapting and expanding the software that controls the Silberfuchs balancing electronic.

Although the first hardware prototype works as intended and is characterized by precise measurement technology and a high degree of efficiency while also requiring little space. However, this electronic unit is not yet designed for series production. The first measurements show that the hardware was able to meet the requirements placed on it. However, individual circuit parts must be optimized to further increase performance and at the same time reduce costs. For example, the use of a circuit board with six copper layers should be considered in order to improve the shielding effect between the power modules and the measurement unit. Furthermore, the two EFD20 inductors could be replaced by a planar transformer and storage choke (cheaper series production), which may require an adjustment of the main switching frequency. In addition, the analog front-end and the digital control system can be revised to achieve a better reaction time and higher accuracy.

8.1 Future works

However, the greatest effort is still in the software. The current prototype uses algorithms/software that was specially written to test the hardware, and therefore only allows rudimentary operations. For example, the selection of the cell as well as the voltage and current set-points must currently be specified by the user. The needed software should therefore be further developed as far as possible for the existing prototype and later adapted to a hardware successor model. A separate research or development project is required to create this software that takes over all functions such as cell selection, measurement, regulation, communication, etc. After this, the process of development a new hardware and adapting the software to this hardware should be accompanied by in-depth tests and measurements directly on a battery stack to get a well-engineered battery management system.

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